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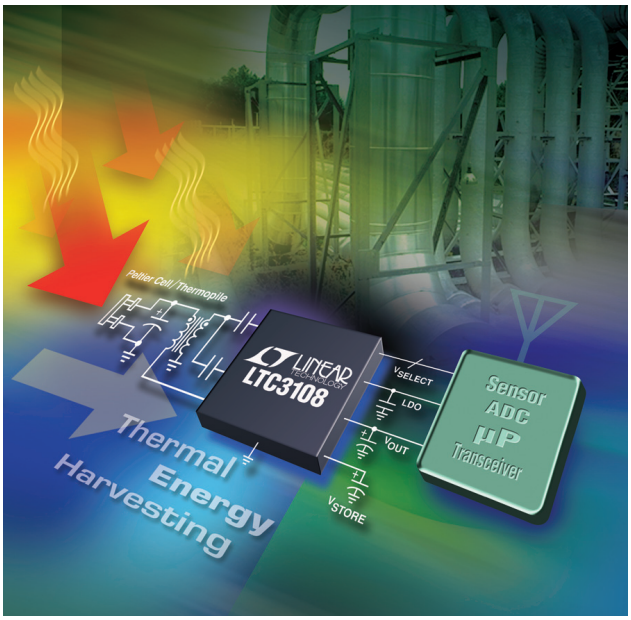
Ultralow Voltage Energy Harvester Uses Thermoelectric Generator for Battery-Free Wireless Sensors

David Salerno

The proliferation of ultralow power wireless sensor nodes for measurement and control, combined with new energy harvesting technology, has made it possible to produce completely autonomous systems that are powered by local ambient energy instead of batteries. Powering a wireless sensor node from ambient or "free" energy is attractive because it can supplement or eliminate the need for batteries or wires. This is a clear benefit when battery replacement or servicing is inconvenient, costly or dangerous.



A complete lack of wires also makes it easy to expand monitoring and control systems on a large scale. Energy harvesting wireless sensor systems simplify installation and maintenance in such diverse areas as building automation, wireless/automated metering and predictive maintenance, as well as numerous other industrial, military, automotive and consumer applications.

The benefits of energy harvesting are clear, but an effective energy harvesting system requires a clever power management scheme to convert the miniscule levels of free energy into a form usable by the wireless sensor system.

IT'S ALL ABOUT THE DUTY CYCLE

Many wireless sensor systems consume very low average power, making them prime candidates to be powered by energy harvesting techniques. Many sensor nodes are used to monitor physical quantities that change slowly. Measurements can therefore be taken and transmitted infrequently, resulting in a low duty cycle of operation and a correspondingly low average power requirement.

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The missing link in the energy harvesting system chain has been the power converter/power management block that can operate from one or more of the common sources of free energy. The LTC3108 and other Linear energy harvesting parts fill in this missing link.

For example, if a sensor system requires 3.3V at 30mA (100mW) while awake, but is only active for 10ms out of every second, then the average power required is only 1mW, assuming the sensor system current is reduced to microamps during the inactive time between transmit bursts. If the same wireless sensor only samples and transmits once a minute instead of once a second, the average power plummets under 20µW. This difference is significant, because most forms of energy harvesting offer very little steady-state power; usually no more than a few milliwatts, and in some cases only microwatts. The less average power required by an application, the more likely it can be powered by harvested energy.

ENERGY HARVESTING SOURCES

The most common sources of energy available for harvesting are vibration (or motion), light and heat. The transducers for all of these energy sources have three characteristics in common:

- Their electrical output is unregulated and doesn't lend itself to being used directly for powering electronic circuits
- They may not provide a continuous, uninterrupted source of power
- They generally produce very little average output power, usually in the range of 10µW to 10mW.

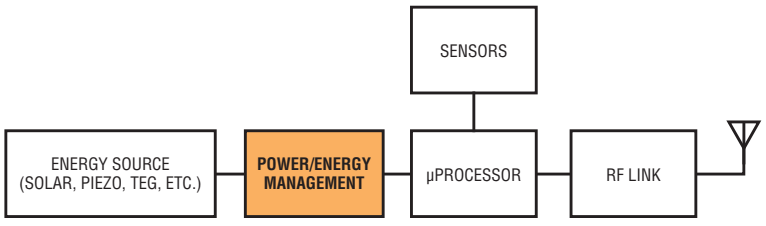
These characteristics demand judicious power management if the source is going to be useful in powering wireless sensors or other electronics.

POWER MANAGEMENT: THE MISSING LINK IN ENERGY HARVESTING—UNTIL NOW

A typical wireless sensor system powered by harvested energy can be broken down into five fundamental blocks, as illustrated in Figure 1. With the exception of the power management block, all of these blocks have been commonly available for some time. For example, microprocessors that run on microwatts of power, and small, cost effective RF transmitters and transceivers that also consume very little power are widely available. Low power analog and digital sensors are also ubiquitous.

(continued on page 4)

Figure 1. Typical wireless sensor block diagram



Linear in the News

ELECTRONICA 2010

The Electronica international trade show will be held in Munich, November 9–12 and Linear will be there to showcase high performance analog solutions for:

- *Automotive:* battery stack monitors, isolated power µModule® products and power management products
- *Industrial:* SAR ADCs, references, ADC drivers, TimerBlox™ timing devices and linear regulators
- *Communications:* µModule receivers, high speed data converters, ADC drivers, filters, dual mixers, I/Q modulators and demodulators, RF power detectors and digital power managers
- *Power Subsystems:* µModule DC/DC regulators

If you're planning to attend Electronica, visit Linear in Hall A4, Booth 538.

LINEAR TECHNOLOGY AT ELECTRONICA 2010
The Electronica international trade show will be held in Munich, November 9–12 and Linear will be there to showcase high performance analog solutions for automotive, industrial, communications and other industries.

ENERGY HARVESTING & WIRELESS SENSOR NETWORK CONFERENCE

Linear will also have booths (21 and 22) at the Energy Harvesting & Wireless Sensor Network Conference, held at the Cambridge Hyatt Regency, Cambridge, Massachusetts, November 16–17. There, Linear will showcase its growing family of energy harvesting products. These innovative devices harvest minute amounts of power from various sources, including solar, vibration and thermal in order to power sensors. These devices can be used in a broad range of applications, including building automation to optimize HVAC system efficiency, aircraft structural monitoring, sensor systems for industrial process control, and for bridge and highway sensor systems.

At the conference, Sam Nork, Director of Linear's Boston Design Center, will speak on "Practical Design Considerations for Piezoelectric Energy Harvesting Applications" at noon on November 16. In his presentation, Sam will discuss how scavenging energy from readily available sources offers the potential to power applications indefinitely without wires or batteries, or to extend the operating times of battery-powered systems. Successful implementation of a vibration energy harvesting solution requires an understanding of the vibration source characteristics and harvester/transducer output power capabilities, as well as insight into the system power needs. This presentation will describe characteristics of piezoelectric and electromagnetic induction generators and provide methods for characterizing a vibration source for peak acceleration and frequency modes. Generator open circuit voltage, maximum power point tracking, and charge storage methods for optimizing available system power will be discussed. Start-up and quiescent power saving strategies will be provided using readily available piezoelectric generators and integrated circuits.

ENERGY HARVESTING PRODUCTS WIN E-LEGACY AWARD

Linear Technology was selected by UK's *Electronic Product Design* magazine as winner of the e-Legacy Alternative Energy Award for the Energy Harvesting product family. The award was presented at the award luncheon in London in September. The award highlighted the LTC®3109 ultralow voltage step-up converter and power manager for harvesting surplus energy from thermoelectric generators. ■

An ideal power management solution for energy harvesting should be small, easy to apply and perform well from the exceptionally high or low voltages produced by common energy harvesting sources.

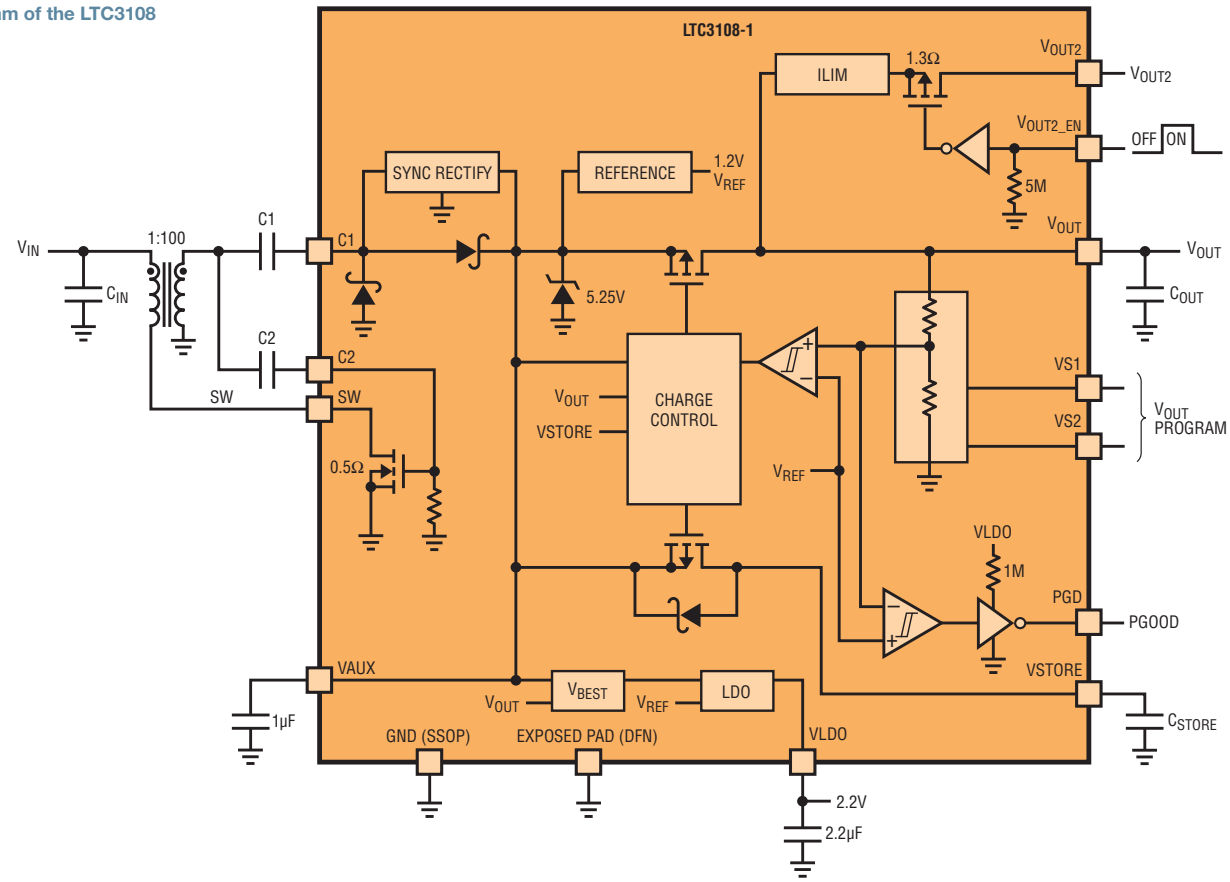
(LTC3108, continued from page 2)

The missing link in completing this energy harvesting system chain has been the power converter/power management block that can operate from one or more of the common sources of free energy. An ideal power management solution for energy harvesting should be small, easy to apply and perform well while operating from the exceptionally high or low voltages produced by common energy harvesting sources, ideally providing a good load match to the source impedance for optimal power transfer. The power manager itself must require very little current to manage the accumulated energy and produce regulated output voltages with a minimal number of discrete components.

The LTC3108, available in either a 3mm × 4mm × 0.75mm 12-pin DFN or 16-pin SSOP package, solves the energy harvesting problem for ultralow input voltage applications. It provides a compact, simple, highly integrated monolithic power management solution for operation from input voltages as low as 20mV. This unique capability enables it to power wireless sensors from a thermoelectric generator (TEG), harvesting energy from temperature differentials (ΔT) as small as 1°C. Using a small (6mm × 6mm), off-the-shelf step-up transformer and a handful of low cost capacitors, it provides the regulated output voltages necessary for powering today's wireless sensor electronics.

The LTC3108 uses a step-up transformer and an internal MOSFET to form a resonant oscillator capable of operating from very low input voltages. With a transformer ratio of 1:100, the converter can start up with inputs as low as 20mV. The transformer secondary winding feeds a charge pump and rectifier circuit, which is used to

Figure 2. Block diagram of the LTC3108



power the IC (via the V_{AUX} pin) and charge the output capacitors. The 2.2V LDO output is designed to be in regulation first, to power a low power microprocessor as soon as possible. After that, the main output capacitor is charged to the voltage programmed by the VS1 and VS2 pins (2.35V, 3.3V, 4.1V or 5.0V) for powering sensors, analog circuitry, RF transceivers or even charging a supercapacitor or battery. The V_{OUT} reservoir capacitor supplies the burst energy required during the low duty cycle load pulse when the wireless sensor is active and transmitting. A switched output (V_{OUT2}), easily controlled by the host, is also provided for powering circuits that don't have a shutdown or low power sleep mode. A power good output is included to alert the host that the main output voltage is close to its regulated value. Figure 2 shows a block diagram of the LTC3108. The LTC3108-1 is identical to the LTC3108 except that it provides a different set of selectable output voltages (2.5V, 3.0V, 3.7V or 4.5V.)

Once V_{OUT} is charged and in regulation, harvested current is diverted to the V_{STORE} pin for charging an optional large storage capacitor or rechargeable battery. This storage element can be used to maintain regulation and power the system in the event that the energy harvesting source is intermittent. The output voltage sequencing during power-up and power-down can be seen in Figure 3. A shunt regulator on the V_{AUX} pin prevents V_{STORE} from charging above 5.3V.

Using a typical 40mm square TEG, the LTC3108 can operate from a ΔT as low as 1°C, making it useful for a wide variety of energy harvesting applications. A higher ΔT results in the LTC3108 being able to supply a higher average output current.

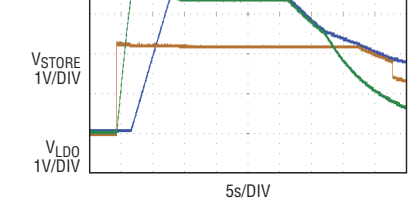


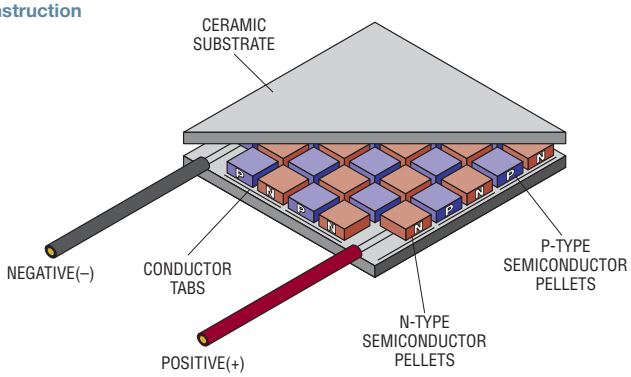
Figure 3. Voltage sequencing during power-up and power-down

TEG BASICS

Thermoelectric generators (TEGs) are simply thermoelectric modules that convert a temperature differential across the device, and resulting heat flow through it, into a voltage via the Seebeck effect. The reverse of this phenomenon, known as the Peltier effect, produces a temperature differential by applying a voltage and is familiarly used in thermoelectric coolers (TECs).The polarity of the output voltage is dependent on the polarity of the temperature differential across the TEG. Reverse the hot and cold sides of the TEG and the output voltage changes polarity.

TEGs are made up of pairs or couples of N-doped and P-doped semiconductor pellets connected electrically in series and sandwiched between two thermally conductive ceramic plates. The most commonly used semiconductor material is bismuth-telluride (Bi_2Te_3). Figure 4 illustrates the mechanical construction of a TEG.

Figure 4. TEG construction



Some manufacturers differentiate between a TEG and a TEC. When sold as a TEG, it generally means that the solder used to assemble the couples within the module has a higher melting point, allowing operation at higher temperatures and temperature differentials, and therefore higher output power than a standard TEC (which is usually limited to a maximum of 125°C). Most low power harvesting applications do not see high temperatures or high temperature differentials.

TEGs come in a wide variety of sizes and electrical specifications. The most common modules are square, ranging in size from about 10mm to 50mm per side. They are usually 2mm–5mm thick.

A number of variables control how much voltage a TEG will produce for a given ΔT (proportional to the Seebeck coefficient). Their output voltage is in the range of 10 mV/K to 50mV/K of differential temperature (depending on the number of couples), with a source resistance in the range of 0.5Ω to 5Ω. In general, the more couples a TEG has in series, the higher its output voltage is for a given ΔT. However, increasing the number of couples also increases the series resistance of the TEG, resulting in a larger voltage drop when loaded. Manufacturers can

A good rule of thumb when selecting a thermoelectric module for power generation purposes is to choose the module with the highest product of (V_{MAX} • I_{MAX}) for a given size.

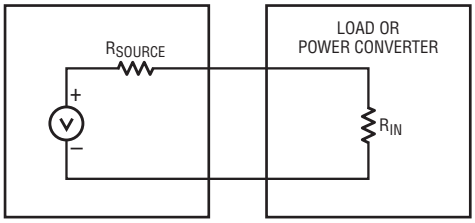


Figure 5. Simplified schematic of a voltage source driving a resistive load

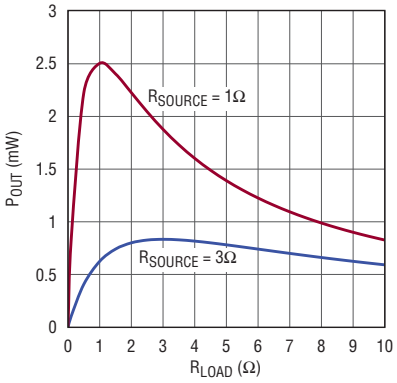


Figure 6. Output power from the source as a function of load resistance

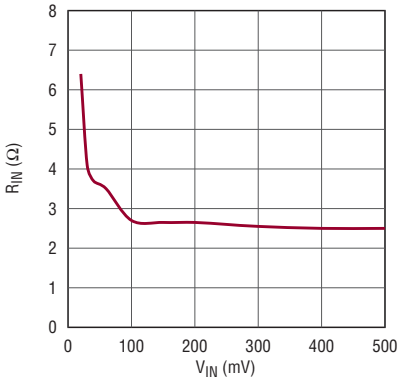


Figure 7. Input resistance vs V_{IN} (1:100 ratio) for the LTC3108

compensate for this by adjusting the size and design of the individual pellets to preserve a low resistance while still providing a higher output voltage.

LOAD MATCHING

To extract the maximum amount of power available from any voltage source, the load resistance must match the internal resistance of the source. This is illustrated in the example of Figure 5, where a source voltage with an open-circuit voltage of 100mV and a source resistance of either 1Ω or 3Ω is driving a load resistor. Figure 6 shows the power delivered to the load as a function of load resistance. It can be seen in each curve that maximum power is delivered to the load when the load resistance matches the source resistance. Nevertheless, it is also important to note that when the source resistance is *lower* than the load resistance, the power delivered may not be the maximum possible but is still higher (1.9mW in this example) than a higher source resistance driving a matched load (0.8mW in this example). This is why choosing a TEG with the lowest electrical resistance provides the most output power.

The LTC3108 presents a minimum input resistance of about 2.5Ω to the input source. (Note that this is the input resistance of the converter, not the IC itself.) This falls in the middle of the range of most TEG source resistances, providing a good load match for nearly optimal power transfer. The design of the LTC3108 is such that as V_{IN} drops, the input resistance increases (shown in Figure 7). This feature allows the LTC3108 to adapt reasonably well to TEGs with different source resistances.

Since the converter input resistance is fairly low, it draws current from the source, regardless of load. For example, Figure 8 shows that with a 100mV input, the converter draws about 37mA from the source. This input current is not to be confused with the 6µA of quiescent current required by the IC itself (off of V_{AUX}) to power its internal circuitry. The low quiescent current is most meaningful during start-up at the minimum voltage, or when operating from a storage capacitor.

CHOOSING A TEG FOR POWER GENERATION

Most thermoelectric module manufacturers do not provide data for output voltage or output power versus differential temperature, which is what the designer of a thermal energy harvester wants to see. Two parameters that are always provided are V_{MAX} and I_{MAX}, which are the maximum operating voltage and maximum operating current for a particular module (when being driven in a heating/cooling application).

A good rule of thumb when selecting a thermoelectric module for power generation purposes is to choose the module with the highest product of (V_{MAX} • I_{MAX}) for a given size. This generally provides the highest TEG output voltage and the lowest source resistance. One caveat to this rule is that the heat sink must be sized according to the size of the TEG. Larger TEGs require larger heat sinks for optimal performance.

The LTC3109 is uniquely suited to the challenge of harvesting energy from sources of either polarity. Using transformers with a step-up ratio of 1:100, it can operate from input voltages as low as ±30mV.

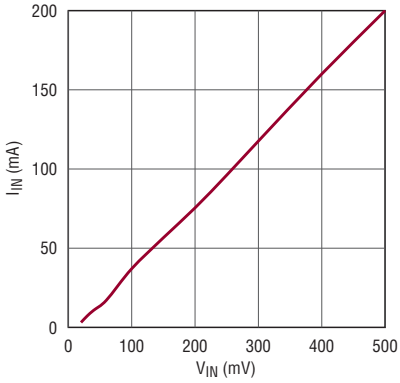


Figure 8. Input current vs V_{IN} (1:100 ratio) for the LTC3108

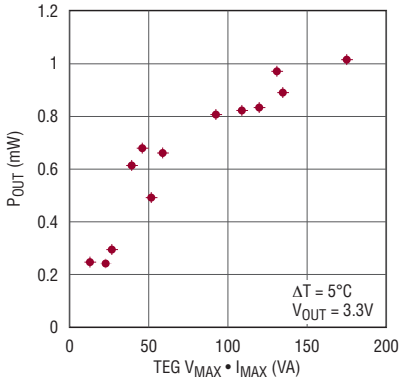


Figure 9. LTC3108 output power vs TEGs with different VI products

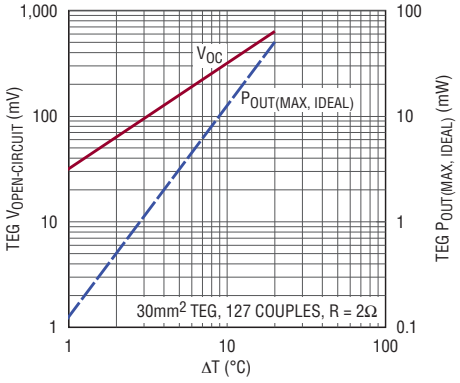


Figure 10. Open-circuit voltage and maximum power output from a typical TEG

Note that the electrical resistance, if given, is specified as an AC resistance because it cannot be measured in the conventional manner using a DC current, as DC current causes a Seebeck voltage to be generated, which yields erroneous resistance readings. Figure 9 is a plot of the power output from the LTC3108 using thirteen different TEGs at a fixed ΔT of 5°C versus the (V_{MAX} • I_{MAX}) product for each module. It can be seen that higher VI products generally result in higher output power from the LTC3108.

Figure 10 shows the output voltage and maximum output power capability for a 30mm square TEG over a ΔT range of 1°C to 20°C. The output power varies from hundreds of microwatts to tens of milliwatts over this range. Note that this power curve assumes an ideal load match, with no conversion losses. Ultimately, the available output power after being boosted to a higher voltage by the LTC3108 is less due to power conversion losses. The LTC3108 data sheet provides several graphs of available output power over several different operating conditions.

The size of the TEG required for a given application depends on the minimum ΔT available, and the maximum average power required by the load, as well as the thermal resistance of the heat sink being used to maintain one side of the TEG at ambient. The maximum power output of the LTC3108 is in the range of 15µW/K-cm² to 30µW/K-cm², depending on transformer turns ratio and the specific TEG chosen. Some recommended TEG part numbers are provided in Table 1.

THERMAL CONSIDERATIONS

When placing a TEG between two surfaces at different temperatures, the "open circuit" temperature differential, before the TEG is added, is higher than the temperature differential across the TEG when it's in place. This is due to the fact that the TEG itself has a fairly low thermal resistance between its plates (typically 1°C/W to 10°C/W).

For example, consider a situation where a large piece of machinery is running with a surface temperature of 35°C and a surrounding ambient temperature of 25°C. When a TEG is attached to the machinery, a heat sink must be added to the cool (ambient) side of the TEG, otherwise the entire TEG would heat up to nearly 35°C, erasing any temperature differential. Keep in mind that it is the heat flow through the TEG that produces electrical output power.

In this example, the thermal resistance of the heat sink and the TEG dictate what portion of the total ΔT exists across the TEG. A simple thermal model of the system is illustrated in Figure 11. Assuming that the thermal resistance of the heat source (RS) is negligible, the thermal resistance of the TEG (RTEG) is 2°C/W, and the thermal resistance of the heat sink is 8°C/W, the resulting ΔT across the TEG is only 2°C. The low output voltage from a TEG with just a few degrees across it highlights the importance of the LTC3108's capability to operate from Ultralow input voltages.

Note that large TEG's usually have a lower thermal resistance than smaller ones due to the increased surface area. Therefore,

in applications where a relatively small heat sink is used on one side of the TEG, a larger TEG may have less ΔT across it than a smaller one, and therefore may not necessarily provide more output power. In any case, using a heat sink with the lowest possible thermal resistance maximizes the electrical output by maximizing the temperature drop across the TEG.

SELECTING THE OPTIMAL TRANSFORMER TURNS RATIO

For applications where higher temperature differentials (i.e. higher input voltages) are available, a lower turns ratio transformer, such as 1:50 or 1:20, can be used to provide higher output current capability. As a rule of thumb, if the minimum input voltage is at least 50mV under load, then a 1:50 ratio is recommended. If the minimum input voltage is at least 150mV, then a 1:20 ratio is recommended. All of the ratios discussed are available as off-the-shelf parts from Coilcraft (please refer to the LTC3108 data sheet for more information, including specific part numbers). The curves in Figure 12 show the output power capability of the LTC3108 over a range of temperature differentials, using two different transformer step-up ratios and two different size TEGs.

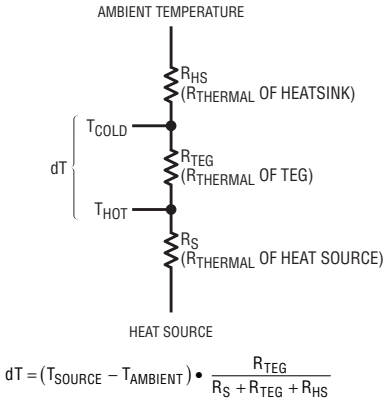


Figure 11. Thermal resistance model of a TEG and heatsink

PULSED LOAD APPLICATION

A typical wireless sensor application powered by a TEG is shown in Figure 13. In this example a temperature differential of at least 2°C is available across the TEG, so a 1:50 transformer ratio was chosen for the highest output power in the range of 2 to 10 degrees ΔT. Using the TEG shown (a 40mm square device with a resistance of 1.25Ω), this circuit can start-up and charge the V_{OUT} capacitor from temperature differentials of as little as 2°C. Note that there is a bulk decoupling capacitor across the input terminals of the converter. Providing good decoupling of the voltage from the TEG minimizes input ripple, improving output power capability and allowing start-up at the lowest possible ΔT.

In the example of Figure 13, the 2.2V LDO output powers the microprocessor, while V_{OUT} has been programmed to 3.3V, using the VS1 and VS2 pins, to power the RF transmitter. The switched V_{OUT} (V_{OUT2}) is controlled by the microprocessor to power 3.3V sensors only when needed. The PGOOD output lets the microprocessor know when V_{OUT} has reached 93% of its regulated value. To maintain operation in the absence of an input voltage, a 0.1F storage capacitor

Table 1. Recommended TEG part numbers by size and manufacturer/distributor

	15MM	20MM	30MM	40MM
CUI INC (Distributor)	CP60133	CP60233	CP60333	CP85438
FERROTEC	9501/031/030 B	9501/071/040 B	9500/097/090 B	9500/127/100 B
FUJITAKA	FPH13106NC	FPH17106NC	FPH17108AC	FPH112708AC
KRYOTHERM			TGM-127-1.0-0.8	LCB-127-1.4-1.15
LAIRD TECHNOLOGY			PT6.7.F2.3030.W6	PT8.12.F2.4040.TA.W6
MARLOW INDUSTRIES		RC3-8-01	RC6-6-01	RC12-8-01LS
TELLUREX	C2-15-0405	C2-20-0409	C2-30-1505	C2-40-1509
TE TECHNOLOGY	TE-31-1.0-1.3	TE-31-1.4-1.15	TE-71-1.4-1.15	TE-127-1.4-1.05

With their unique ability to operate at input voltages as low as 20mV, or from very low voltages of either polarity, the LTC3108 and LTC3109 provide simple, effective power management solutions that enable thermal energy harvesting for powering wireless sensors and other low power applications from common thermoelectric devices.

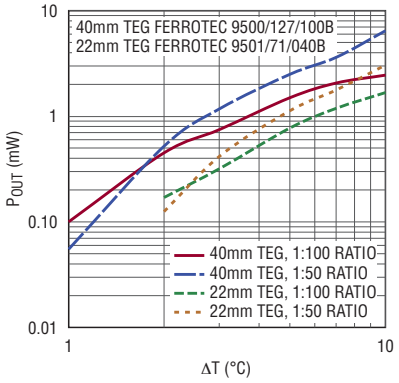


Figure 12. LTC3108 output power vs ΔT for two sizes of TEG and two transformer ratios for V_{OUT} = 5V

is charged in the background from the V_{STORE} pin. This capacitor can charge all the way up to the 5.25V clamp voltage of the V_{AUX} shunt regulator. In the event that the input voltage source is lost, energy is automatically supplied by the storage capacitor to power the IC and maintain regulation of V_{LDO} and V_{OUT} .

In this example, the C_{OUT} reservoir capacitor has been sized to support a total load pulse of 15mA for a duration of 10ms, allowing for a 0.33V drop in V_{OUT} during the load pulse, according to the formula below. Note that I_{PULSE} includes loads on V_{LDO} and V_{OUT2} as well as V_{OUT}, and that charging current available is not included, as it may be very small compared to the load.

$$C_{OUT}(\mu F) = \frac{I_{PULSE}(mA) \bullet t_{PULSE}(ms)}{dV_{OUT}}$$

Given these requirements, C_{OUT} must be at least 454µF, so a 470µF capacitor was selected.

With the TEG shown, operating at a ΔT of 5°C, the average charge current available from the LTC3108 at 3.3V is about 560µA. With this information, we can calculate how long it takes to charge the V_{OUT} reservoir cap the first time, and how frequently the circuit can transmit a pulse. Assuming the load on V_{LDO} and V_{OUT} is very small (relative to 560µA) during the charging phase, the initial charge time for V_{OUT} is:

$$t_{CHARGE} = \frac{470\mu F \bullet 3.3V}{560\mu A} = 2.77 \text{ seconds}$$

Assuming that the load current between transmit pulses is very small, a simple way to estimate the maximum transmit rate allowed is to divide the average output power available from the LTC3108, in this case 3.3V • 560µA = 1.85mW, by the power required during a pulse, in this case 3.3V • 15mA = 49.5mW. The maximum duty cycle that the harvester can support is 1.85mW/49.5mW = 0.037 or 3.7%. Therefore the maximum transmit burst rate is 0.01/0.037 = 0.27 seconds or about 3.7Hz.

Keep in mind that if the average load current (as determined by the transmit rate) is the highest that the harvester can support, there will be no harvested energy left over to charge the storage capacitor (if storage capability is desired). Therefore, in this example the transmit rate is set to 2Hz, leaving almost half of the available energy to charge the storage capacitor. In this case, the storage time provided by the V_{STORE} capacitor is calculated using the following formula:

$$t_{STORE} = \frac{0.1F \bullet (5.25V - 3.3V)}{6\mu A + 15mA \bullet \frac{0.01}{0.5}} = 637 \text{ seconds}$$

This calculation includes the 6µA quiescent current required by the LTC3108, and assumes that the loading between transmit pulses is extremely small. In this case, once the storage capacitor reaches full charge, it can support the load for 637 seconds at a transmit rate of 2Hz, or a total of 1274 transmit bursts.

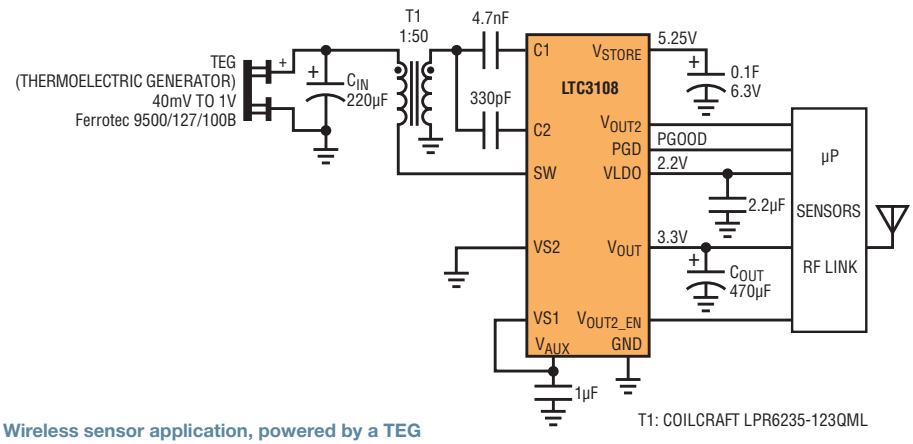


Figure 13. Wireless sensor application, powered by a TEG

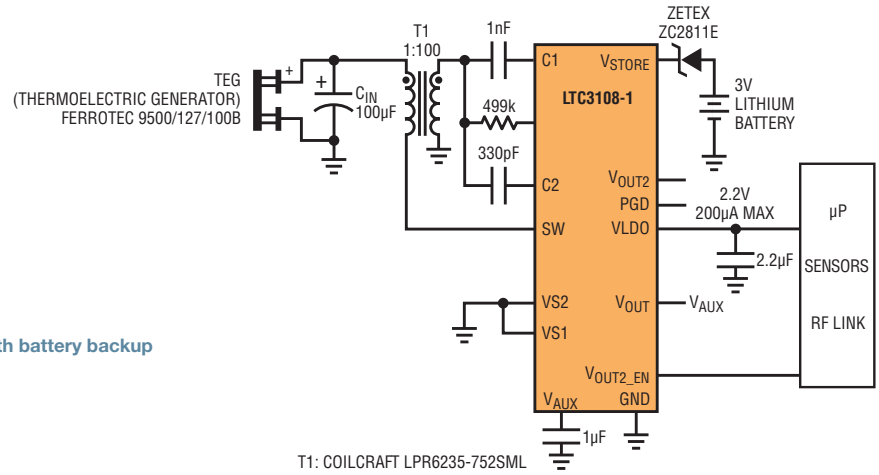


Figure 14. Energy harvester with battery backup

ULTRALOW POWER APPLICATION WITH BATTERY BACKUP

Some applications may not have a pulsed load, but may operate continuously. Such applications are traditionally powered by a small primary battery, such as a 3V lithium coin cell. If the power demand is low enough these applications can be powered continuously by thermal harvesting, or may use thermal harvesting to greatly extend the life of the battery, reducing maintenance costs.

Figure 14 shows an energy harvesting application with battery backup to drive a continuous load. In this example, where all the electronics are powered entirely from the 2.2V LDO output and consume less than 200µA total, the LTC3108 can power the load continuously as long as a temperature differential of at least 3°C exists across the TEG. Under these conditions, there is no load on the battery. For times when there is insufficient harvested energy available, the 3V lithium battery seamlessly takes over and powers the load.

ENERGY STORAGE ALTERNATIVES

For applications that choose to use a rechargeable battery instead of a primary battery for backup or energy storage, the diode in Figure 14 can be removed and the lithium battery can be replaced by a nickel-based rechargeable or a Li-ion battery (including the new thin-film lithium rechargeables). If a nickel-based rechargeable battery is used, its self-discharge current must be smaller than the average charge current the LTC3108 can provide. If a Li-ion battery is chosen, additional circuitry is required to protect it from over-charge and over-discharge. Yet another storage alternative would be a supercapacitor with a 5.25V rating, such as the Cooper-Bussman PB-5R0H104-R. Supercapacitors offer the benefit of a higher number of charge/discharge cycles than rechargeable batteries but have much lower energy density.

Figure 15. Autopolarity energy harvester-powered wireless sensor node

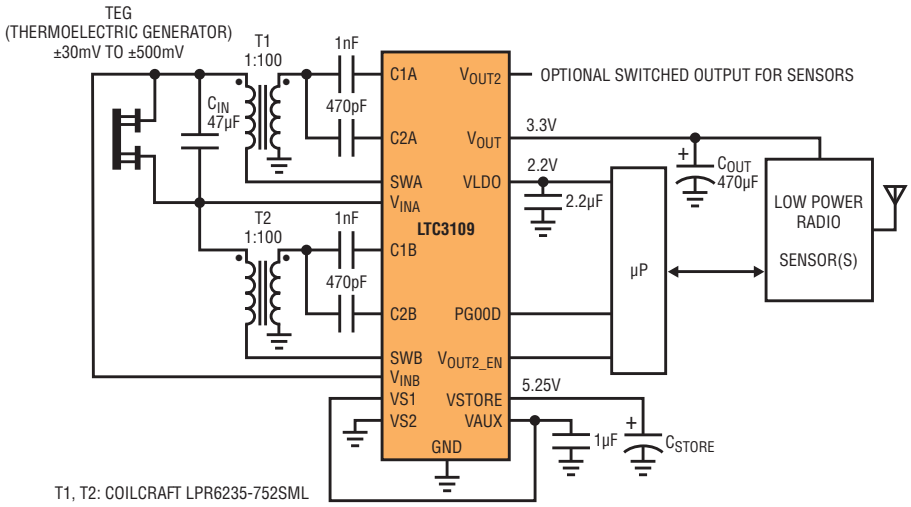
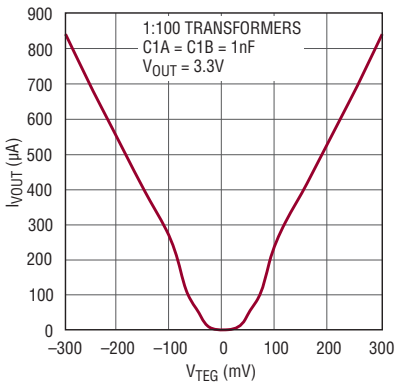


Figure 16. Output current vs Vin for the converter in Figure 15



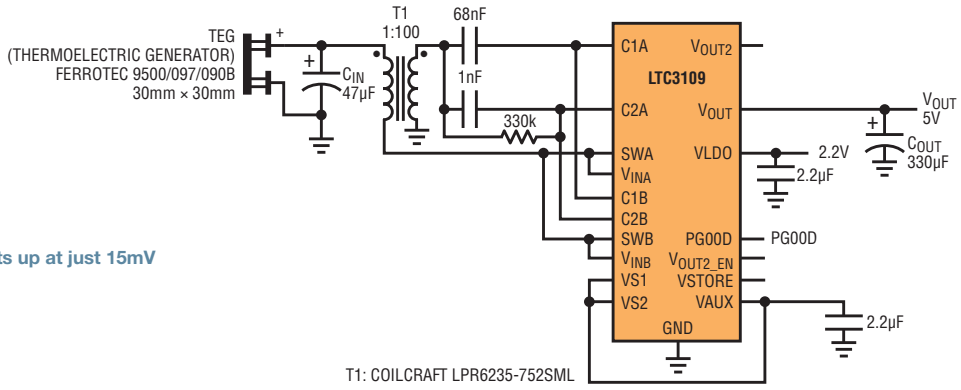


Figure 17. Unipolar converter using the LTC3109 starts up at just 15mV

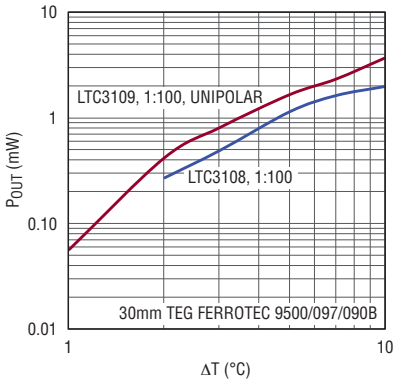
THERMAL HARVESTING APPLICATIONS REQUIRING AUTOPOLARITY

Some applications, such as wireless HVAC sensors or geothermal powered sensors present another unique challenge to an energy harvesting power converter. These applications require that the energy harvesting power manager be able to operate not only from a very low input voltage, but one of either polarity as the polarity of the ΔT across the TEG changes. This is a particularly challenging problem, and at voltages in the tens or hundreds of millivolts, diode bridge rectifiers are not an option.

The LTC3109 is uniquely suited to the challenge of harvesting energy from sources of either polarity. Using transformers with a step-up ratio of 1:100, it can operate from input voltages as low as ±30mV. The LTC3109 offers the same feature set as the LTC3108, including an LDO, a digitally programmable output voltage, a power good output, a switched output and an energy storage output. The LTC3109 is available in either a 4mm × 4mm 20-pin QFN package or a 20-pin SSOP package. A typical example of the LTC3109 being used in an autopolarity application is shown in Figure 15. Output current vs V_{IN} curves for the converter are shown in Figure 16, and illustrate the ability to function equally well from input voltages of either polarity.

The LTC3109 can also be configured for unipolar operation, using a single transformer (like the LTC3108) to satisfy those applications requiring the lowest possible startup voltage and the highest possible output current. The circuit shown in Figure 17 starts up at just 15mV, which occurs at a differential temperature of less than 1°C using the TEG shown. At a temperature differential of 10°C it can deliver a regulated 5V at 0.74mA for 3.7mW of regulated steady state output power. This is almost double the output power of the LTC3108 under the same conditions, as shown in Figure 18.

Figure 18. Comparison of LTC3108 output with LTC3109 output in unipolar configuration



Note that in the unipolar configuration, the LTC3109 presents a load resistance of about 1Ω to the TEG, so it's important to choose a TEG with very low source resistance for good load matching, otherwise there will be no benefit to using the LTC3109 in a unipolar configuration. The TEG used in this example has a nominal source resistance of 1.0Ω for optimal power transfer.

CONCLUSION

With their unique ability to operate at input voltages as low as 20mV, or from very low voltages of either polarity, the LTC3108 and LTC3109 provide simple, effective power management solutions that enable thermal energy harvesting for powering wireless sensors and other low power applications from common thermoelectric devices. Available in either a 12-pin DFN or 16-pin SSOP package (LTC3108 and LTC3108-1), and 20-pin QFN or SSOP packages (LTC3109), these products offer unprecedented low voltage capabilities and a high level of integration to minimize the solution footprint. The LTC3108, LTC3108-1 and LTC3109 interface seamlessly with existing low power building blocks to support autonomous wireless sensors and extend the battery life in critical battery backup applications. ■

POL µModule DC/DC Converter Operates from Inputs Down to 1.5V, Delivering Up to 15A Output, Without an Auxiliary Bias Supply

Jason Sekanina and Alan Chern

The LTM4611 is a low profile µModule step-down switch mode DC/DC converter in a compact 15mm × 15mm × 4.32mm LGA surface mount package. The switching controller, MOSFETs, inductor and support components are housed in the package, so design is reduced to selecting a few external components. The LTM4611 operates from an input voltage of 1.5V to 5.5V (6V, absolute maximum), making it suitable for a variety of power architectures—particularly data storage and RAID (redundant array of independent disks) systems, ATCA (advanced telecommunications computing architecture) and networking cards—where one or several commonly bussed voltages are 5V, 3.3V, 2.8V, and/or 2.5V.

While it is uncommon to see bus voltages lower than 2.5V due to the distribution losses (voltage drops) associated with relatively high bus currents, the ability of the LTM®4611 to deliver full power to its load from a 1.5V input is particularly advantageous in applications where load voltage(s) must be precisely regulated even as momentary or sustained electrical events induce input-bus line-sag. Transient events on the system bus can occur normally due to the operation of motors, transducers, defibrillators or an uptick in microprocessor activity. Fault events on a system's distributed bus may leave the bus voltage compromised, but still above 1.5V. The LTM4611's ability to deliver full power from as low as 1.5V input allows it to be considered for mission-critical medical and industrial instruments that have the highest standards for uptime and bus-sag ride-through capability. Precision-regulated power can even be provided by the LTM4611 to its load during so-called "dying-gasps"—sudden, unexpected loss of system power, such as those monitored by utility smart meters—where it is highly desirable to be able to operate from the decaying voltage provided by backup-batteries or supercapacitors for as long as possible.

There is another advantage in the LTM4611's ability to operate from as low as 1.5V: as the number of rails increases in today's power system, so are the number of layers of copper in printed circuit boards (PCBs) required to route (distribute) the power effectively to the load. Consider a hypothetical example: it can be difficult to impossible to route a distributed 5V rail to both 5V-to-1.5V and 5V-to-1.2V DC/DC converters without increasing the number of layers of copper in the PCB. Alternatively, one LTM4611 could convert the 5V rail to a distributed 1.5V copper plane, while another LTM4611 could efficiently convert the 1.5V bus voltage to 1.2V at the POL. The resulting total solution size on the motherboard could be quite compelling, while eliminating the need to route 5V potential to an entire section of the PCB. The option to minimize the number of layers of copper in the manufacture of the PCB has potential for cost and material savings, and associated benefits to PCB yield in mass-production and PCB reliability.

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This particular code, like its clone on the cover, links to the mobile version of the LTM4611 web page at m.linear.com/4611. Most smart phones support QR Code scanning using their built-in cameras. Some phones may require that you download a QR Code scanner/reader application. Look through this article for a few more codes that link to informative videos.

BRAINS AND BRAWN

The muscle behind the LTM4611 is a buck-converter topology that steps down its input voltage to deliver as low as 0.8V, up to 15A continuous, to its output. A voltage drop less than 0.3V from input-to-output and at 15A load is achievable, with proper selection of input-power-source (dynamic characteristic and transient load response) and local bypass capacitance.

SELF-GENERATED BIAS SUPPLY

Another noteworthy feature is that the LTM4611 does not require an auxiliary bias supply to power its internal control IC or MOSFET-drive circuitry; it generates its own low power bias from the input-source

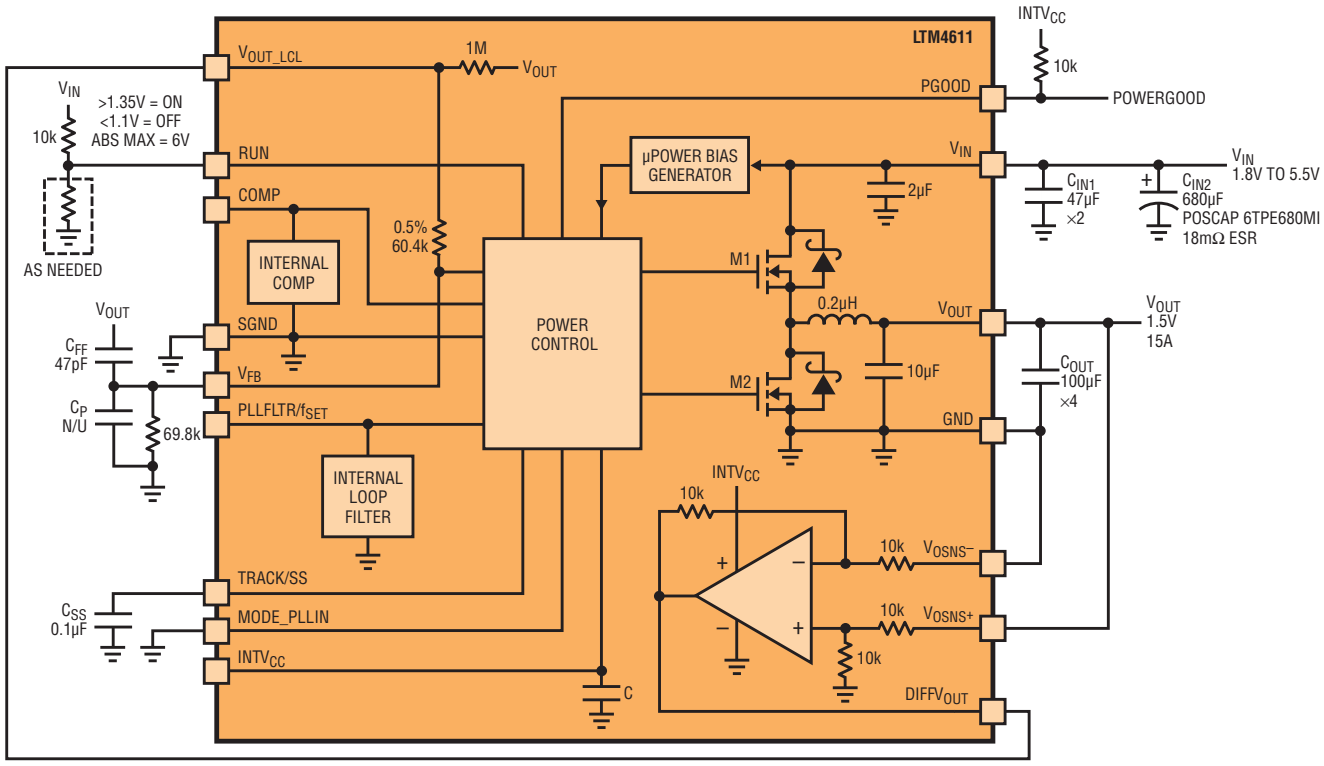


Figure 1. Simplified block diagram of the LTM4611, and typical application

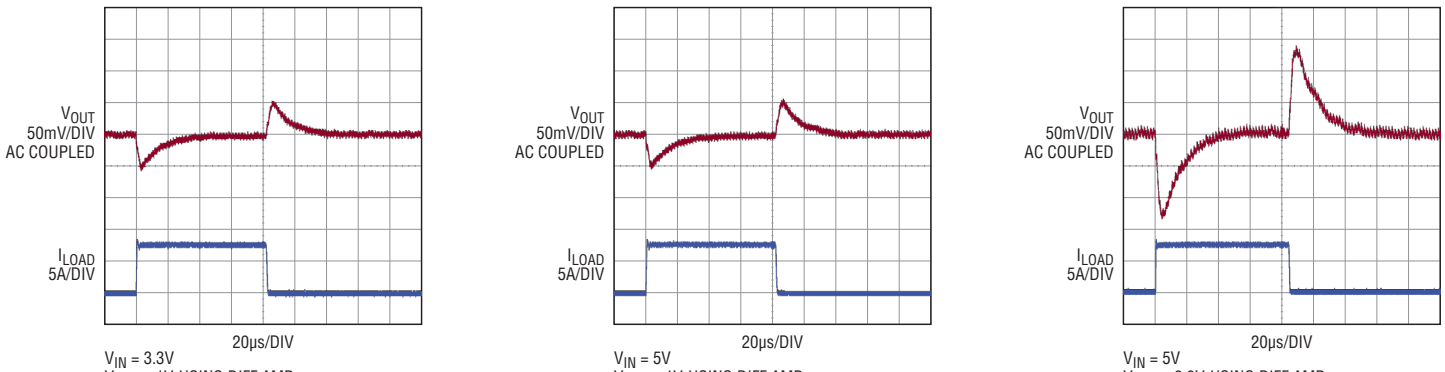
supply. The LTM4611 employs a fixed-frequency peak-current-mode control buck-converter scheme, operating at 500kHz by default. The switching frequency can be adjusted between recommended values of 330kHz to 780kHz with resistor-pin strapping to the PLLFLTR/f_{SET} pin of the LTM4611, or synchronized between 360kHz and 710kHz to a clock signal applied to the MODE_PLLIN pin.

CURRENT SHARING OF MULTIPLE SUPPLIES FOR 60A OR MORE

Current sharing of four modules is supported for solutions up to 60A output. More modules can be paralleled for even higher output current—call the factory for details. Current mode control makes current sharing of modules especially reliable and easy to implement, and ensures module-to-module sharing of current during start-up, transient and steady-state operating conditions.

This is in contrast to many voltage mode modules, which achieve current-sharing by employing either master-slave configurations or by using "droop-sharing" (also called "load-line sharing"). Master-slave configurations can be vulnerable to nuisance overcurrent-tripping during

Figure 2. A sampling of the LTM4611's output voltage transient load responses



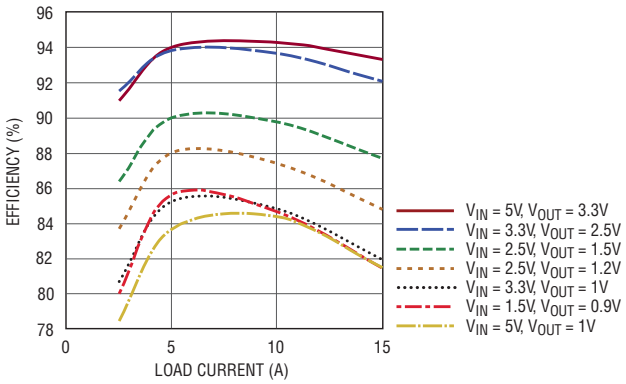


Figure 3. LTM4611 efficiency vs load current for various input and output voltages

Video at video.linear.com/56 shows the test method used to produce Figure 3.

start-up and transient load conditions, while droop-sharing results in compromised load regulation specifications while offering little assurances of good module-to-module current matching during transient load steps.

The LTM4611 typically provides better than 0.2% load regulation from no load to full load—0.5% maximum over the full internal module temperature range of –40°C to 125°C.

EASY POL APPLICATION: 1.8V–5.5V INPUT TO 1.5V OUTPUT AT 15A

The block diagram in Figure 1 shows the LTM4611 operating from 1.8V-to-5.5V input and delivering 1.5V output at 15A. The output voltage is programmed by a single resistor from V_{FB} to GND. The control loop drives the power MOSFETs and output voltage such that V_{FB} is equal to the lesser of 0.8V or the voltage on the TRACK/SS pin. A soft-start capacitor, C_{SS}, on the TRACK/SS pin programs the start-up rate of the LTM4611's output when the module's RUN pin exceeds 1.22V (±10%). C_{SS} assures monotonic output voltage waveform start-up and supports smooth power-up into pre-biased output voltage conditions. A resistor-divider from another rail can be applied to the TRACK/SS pin to program coincident or ratiometric tracking of the LTM4611's output rail to the reference rail. This is a handy feature when powering digital devices with stringent rail-tracking requirements during system power-up and power-down.

PROGRAMMABLE UNDERVOLTAGE LOCKOUT WITH PROGRAMMABLE RISING AND FALLING THRESHOLDS

The resistor-divider (R1/R2) from the input-source (V_{IN}) to the RUN pin of the LTM4611 programs the UVLO (undervoltage lock out) rising and falling thresholds of the DC/DC µModule converter. This ensures that the converter does not draw current from V_{IN} until the input (bus) voltage exceeds the minimum DC voltage, and also programs the hysteresis voltage—the amount of input voltage sag at which the DC/DC converter ceases to regulate (shuts off power to) its output. For minimum component-count and default 80mV hysteresis, connect RUN to V_{IN}, directly. The use of R1 without R2 yields the minimum possible start-up voltage (~1.22V, typical) and allows programming of the turn-off hysteresis.

The role of UVLO is important in all power supply conversion applications, including ultralow V_{IN} DC/DC converter applications that operate at high duty-cycle. Input-referred transient currents that flow as a result of the DC/DC converter responding to transient load steps on its output must be absorbed by the source supply and the input (bus) capacitance, where the combination of a sluggish source supply and insufficient bus bypass capacitance is a recipe for undesirable power supply motor boating during power-up into heavy loads.

EASY LOOP COMPENSATION

The LTM4611 control loop is internally compensated to yield a stable system with a wide assortment of output capacitors. Nevertheless—especially when using low leakage, low ESR, high reliability X5R- or X7R-material ceramic capacitors on the output—transient response can be further improved with a small signal capacitor from V_{OUT} to V_{FB} (C_{FF}), and/or a small signal capacitor from V_{FB} (C_P) to SGND may be warranted to guarantee control loop stability, accounting for ceramic capacitor value variation and ESR variation over age, temperature, and capacitor process.

The LTM4611 data sheet and Linear's simulation design and modeling tools, such as LTspice® and the LTpowerCAD™, take the guesswork out of the loop-stability and transient-load response optimization process. Figure 2 shows transient load response of the LTM4611 for some typical 1V output and 3.3V output applications and data sheet-endorsed ceramic-only output capacitance.

REMOTE SENSING FOR ACCURATE POL REGULATION

Routinely, high current low voltage FPGAs, ASICs, µPs, etc., require extremely accurate voltages of ±3% of nominal V_{OUT} (or better) regulated exactly at the POL terminals

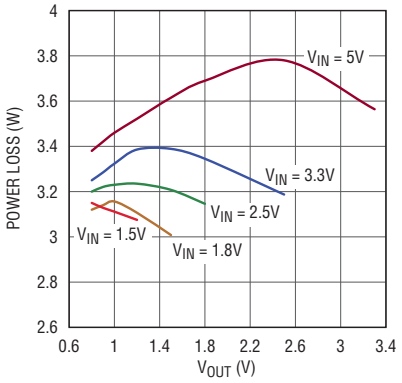


Figure 4. LTM4611 power loss at full load for various input and output voltages

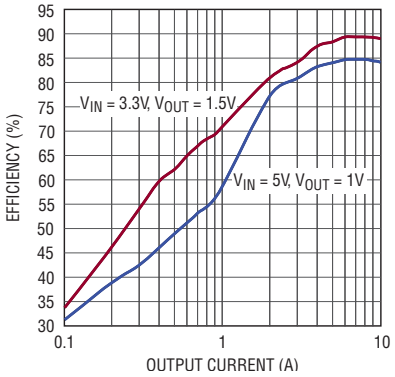


Figure 5. LTM4611 pulse-skipping mode efficiency

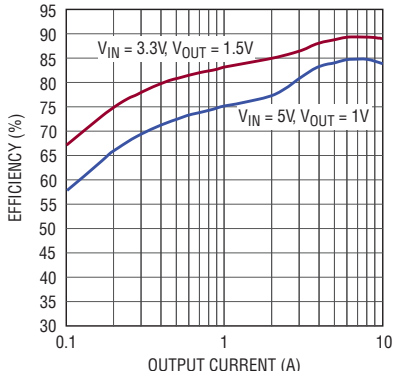


Figure 6. LTM4611 Burst Mode operation efficiency

(e.g. V_{DD} and DGND pins). To meet this regulation requirement where it is hardest to do so—for low output voltages (≤3.7V)—the LTM4611 provides a unity gain buffer for remote sensing of the output voltage at the load's terminals.

Voltage drops across the V_{OUT} and GND copper planes in the PCB are an unavoidable result of resistive distribution losses physically between the module and the load. In Figure 1, it can be seen that the differential feedback signal across the POL (V_{OSNS}+ minus V_{OSNS}–) is reconstructed at DIFF_V_{OUT} with respect to the module's local ground, SGND, thus allowing the control loop to compensate for any voltage drop in the power-delivery path between the module's output pins and the POL device.

The LTM4611 includes an output voltage power good (PGOOD) indicator pin that supplies a logic high open-drain signal when output voltage is within ±5% of nominal V_{OUT}; otherwise, PGOOD pulls logic low. The LTM4611 provides foldback current-limiting to protect itself and upstream power sources from fault conditions on its output. The LTM4611 also includes an overvoltage protection feature: when the output voltage exceeds 107.5% of nominal, the internal low side MOSFET is turned on until the condition is cleared.

LIGHT LOAD OPERATING MODES TO IMPROVE EFFICIENCY OR MINIMIZE RIPPLE

Lastly, the LTM4611 supports forced continuous mode (FCM), pulse-skipping mode (PSM) and Burst Mode® operation schemes, depending on the efficiency and ripple requirements of the application at light loads. These modes are selected by terminating the MODE_PLLIN to GND, pulling it to $INTV_{CC}$ or leaving it floating, respectively. At relatively heavy load currents (>3A), one does not see any difference in module behavior between these three modes—the difference is in light load performance.

At light loads (<3A), in FCM, the power MOSFETs are forced to operate synchronously every switching cycle—energy flow between input source and output load is bidirectional—to minimize inductor ripple current and therefore output voltage ripple. In pulse-skipping operation, energy flow is unidirectional—from input to output, only—and the top MOSFET can turn off for multiple switching cycles at light loads. PSM allows slightly higher efficiency at lighter loads (<3A)—due to decreased switching losses—and yields output voltage ripple and transient load response on par with FCM operation. Pulse-skipping mode accomplishes what is also referred to as "diode emulation" in the industry—making the low side MOSFET behave as an ideal diode (a diode with very low forward voltage drop).

By far the highest efficiency at very light load currents (<1A) can be achieved by utilizing Burst Mode operation, in which buckets of energy are transferred only as needed. Energy flows unidirectionally from input to output, and the output is regulated in a hysteretic fashion, where the LTM4611 resides in a lower-power sleep state and does not resume transfer of energy to the output until the output voltage decays according to whatever light load current is drawn from the output capacitors. Although Burst Mode operation yields higher power conversion efficiency than PSM or FCM at very light loads, the hysteretic control does result in higher output voltage ripple and generates more radiated EMI (electromagnetic interference) in the proximity of the µModule regulator. This should be taken into consideration for proper operation of nearby high speed digital circuits, as well as any EMI regulatory requirements. An LC or so-called π filter may be needed on the input of the LTM4611 to keep EMI to acceptable levels.

HOW GREEN IS YOUR MACHINE?

DC/DC power conversion efficiency and thermal management is as important today, as ever. The LTM4611 provides compelling efficiency in a small land pattern (only 15mm × 15mm) and low physical

The LTM4611's LGA packaging allows heat sinking from both the top and bottom, facilitating the use of a metal chassis or a BGA heat sink. This form factor promotes excellent thermal dissipation with or without airflow.

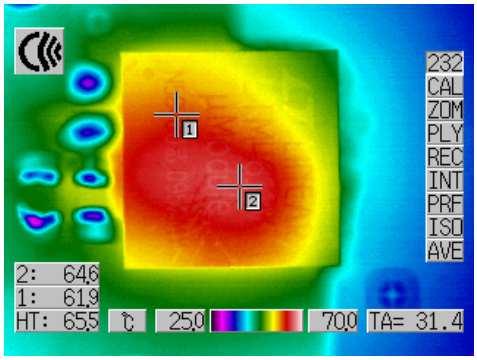


Figure 7. Top thermal image of an LTM4611 regulator producing 1.5V at 15A from at 5V Input. Power loss is 3.5W. No-airflow bench testing results in a 65°C surface temperature hotspot.

Video at video.linear.com/55 shows the test method used to produce Figure 8, and the effect of adding 200 LFM of airflow across the top of the LTM4611.

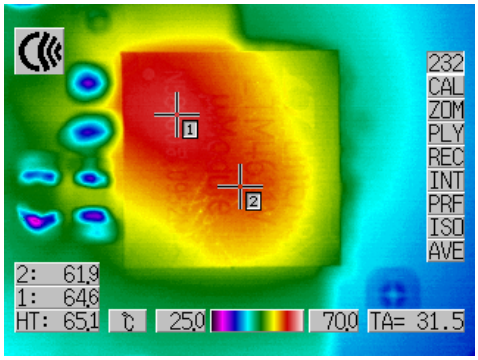


Figure 8. Top thermal image of an LTM4611 regulator producing 1.5V at 15A from at 1.8V Input. Power loss is 3.2W. No-airflow bench testing results in a 65°C surface temperature hotspot.

volume (at only 4.32mm tall—it occupies only one cubic centimeter), in a thermally enhanced LGA (land grid array) package. Figure 3 shows the LTM4611 efficiency for various combinations of input and output voltage conditions. Figure 4 shows full-load power loss versus output voltage for various input voltage conditions. Besides high efficiency, the power dissipation envelope of the LTM4611 is relatively flat for a given input voltage condition, which makes the thermal design and reuse of the LTM4611 in follow-on products easy—even as rail voltages migrate to lower values due to IC die shrink.

For an increasing number of applications, reducing power loss at light loads is as important—if not more important—than reducing power loss at heavy loads. Digital devices are being increasingly, deliberately designed to operate in lower-power states for as long as possible and whenever practical (for energy conservation), and draw peak power (full load) only intermittently. Figures 5 and 6 show the efficiency benefits of operating in PSM and Burst Mode operation at lighter load currents (<3A).

THERMALLY ENHANCED PACKAGING

The device's LGA packaging allows heat-sinking from both the top and bottom, facilitating the use of a metal chassis or a BGA heat sink. This form factor promotes excellent thermal dissipation with or without airflow. Figure 7 shows an infrared (IR) thermal image of the top of the LTM4611 demonstrating a power-loss of 3.5W with no airflow, tested on a lab bench, converting a 5V input to a 1.5V output at 15A. The hottest surface temperature measures around 65°C.

In contrast to Figure 7, Figure 8 shows an IR thermal image of the top of the LTM4611 demonstrating a power loss of only 3.2W with no airflow, tested on a lab bench, converting a 1.8V input to a 1.5V output at 15A. Hotspot *locations*, not their magnitude, are slightly changed from the positions seen during operation at 5V input.

At a low input voltage of 1.8V, conventional monolithic power IC solutions would struggle to deliver satisfactory gate drive amplitude to the power MOSFETs; one's expectations of thermal performance would be lower than what the LTM4611 is able to deliver in Figure 8, thanks to its internal micropower bias generator.

CONCLUSION

The LTM4611 is a µModule buck regulator that easily fits into point-of-load applications needing high output current from low voltage inputs—down to 1.5V. Efficiency and thermal performance remain high across the entire input voltage range, simplifying placement in POL applications. ■

4- and 6-Supply Monitors Feature ±1.5% Accuracy and Watchdog Timers for Rails Down to 1.2V

A. Ng

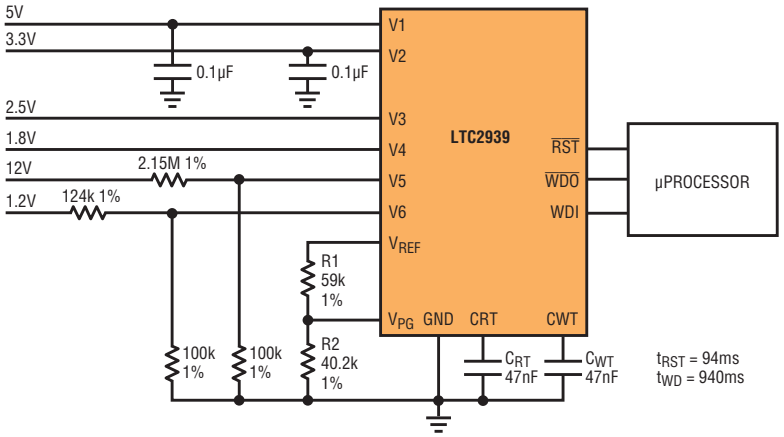
Two new power supply monitors from Linear Technology, the LTC2938 and LTC2939, are specifically designed to monitor lower supply voltages (down to 1.2V) in multivoltage systems. The LTC2938 and LTC2939 share the same architecture and differ only in the number of voltages monitored. The LTC2938 is a 4-supply monitor and comes in compact 12-pin MSOP and DFN packages. The LTC2939 monitors six supplies and is offered in a 16-pin MSOP package. Both monitors have a tight threshold accuracy of 1.5% over the operating temperature range, which eases the voltage headroom requirements of circuits powered by the monitored supplies and is much tighter than supply monitors from other manufacturers. Neither monitor requires external calibration or trimming. Both parts are designed for systems with 5% power supply tolerance.

The watchdog circuit in these monitors includes a watchdog input (WDI) and a watchdog output ($\overline{\text{WDO}}$), which facilitates microprocessor monitoring and control. The $\overline{\text{WDO}}$ output is latched low in the event of a watchdog timeout and allows the microprocessor to distinguish between resets caused by a supply undervoltage from those due to software malfunction. Both devices feature reset and watchdog timers that can be arbitrarily adjusted using external capacitors for greater flexibility in system design.

SINGLE PIN SELECTS FROM 16 POSSIBLE THRESHOLD COMBINATIONS

A single pin (V_{PG}) allows the selection of one of 16 possible threshold configurations. This programmability eliminates the need to qualify, source and stock unique part numbers for different threshold voltage combinations. Figure 1 shows a typical application of the LTC2939 monitoring 12V, 5V, 3.3V, 2.5V, 1.8V and 1.2V supplies with no external resistive dividers required for V1 through V4.

Figure 1. Typical application using the LTC2939 to monitor 6 supply voltages



The LTC2938 and LTC2939 supply threshold voltages are configured by an external resistive divider from the V_{REF} pin to ground (see Figure 2). The center tap of the divider drives the V_{PG} pin. During power-up, the voltage at the V_{PG} pin is detected and used to select one of 16 possible configurations as shown in Table 1. Recommended ±1% resistor values to select each configuration can also be found in Table 1.

The actual supply thresholds are set by integrated precision dividers for 5V, 3.3V, 2.5V, 1.8V, 1.5V and 1.2V supply monitoring. For modes 6 (see Figure 1), 7 and 10, no external resistors are needed at the comparator inputs (V1 through V4) to monitor the combinations of voltages shown in Table 1. For other supply combinations, uncommitted comparators (in ADJ mode) with 0.5V thresholds allow virtually any positive supply to be monitored as shown in Figure 3. The V4 input also monitors negative voltages with the same 1.5% accuracy using the integrated buffered reference for offset (see Figure 4). The LTC2939 has two additional uncommitted

A single pin (V_{PG}) allows the selection of one of 16 possible threshold configurations. This programmability eliminates the need to qualify, source and stock unique part numbers for different threshold voltage combinations.

comparators with 0.5V thresholds for systems that need to monitor up to six supplies. All uncommitted inputs (V3 through V6) can be disabled by tying them to V1.

TIGHT THRESHOLD ACCURACY PREVENTS NUISANCE RESETS AND SYSTEM MALFUNCTIONS

Consider a 5V system with ±5% supply tolerance. The 5V supply may vary between 4.75V to 5.25V. System ICs powered by this supply must operate reliably within this band (and a little more, as explained below). A perfectly accurate supervisor for this supply generates a reset at exactly 4.75V. However, no supervisor is perfect. The actual reset threshold of a supervisor fluctuates over a specified band; the LTC2938 and LTC2939 vary ±1.5% around their nominal threshold voltage over temperature (Figure 5). The reset threshold band and the power supply tolerance bands should not overlap. This prevents false or nuisance resets when the power supply is actually within its specified tolerance band.

The LTC2938 and LTC2939 boast a ±1.5% reset threshold accuracy, so a "5%" threshold is usually set to 6.5% below the nominal input voltage. Therefore, a typical 5V, "5%" threshold is 4.675V. The threshold is guaranteed to lie in the band between 4.750V and 4.600V over temperature. The powered system must work reliably down to the low end of the threshold band, or risk malfunction before a reset signal is properly issued. A less accurate monitor increases the required system voltage margin and increases the probability of system malfunction. The tight ±1.5% accuracy specification of the LTC2938 and LTC2939 improves the reliability of the system over monitors with wider threshold specifications.

Table 1. Voltage threshold modes

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	V_{PG}/V_{REF}
0	5.0	3.3	ADJ	ADJ	Open	Short	0
1	5.0	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	1.8	1.5	ADJ	71.5	28	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59	40.2	0.406
7	3.3	1.8	1.5	1.2	53.6	47.5	0.469
8	3.3	1.8	1.2	ADJ	47.5	53.6	0.531
9	3.3	1.8	ADJ	ADJ	40.2	59	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28	71.5	0.719
12	3.3	1.8	ADJ	–ADJ	22.1	78.7	0.781
13	3.3	1.5	ADJ	ADJ	16.2	86.6	0.844
14	5	3.3	1.8	ADJ	9.53	93.1	0.906
15	3.3	1.2	ADJ	ADJ	Short	Open	1

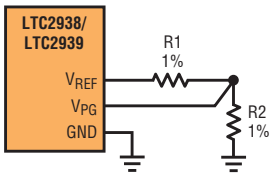


Figure 2. Programming the voltage monitoring mode

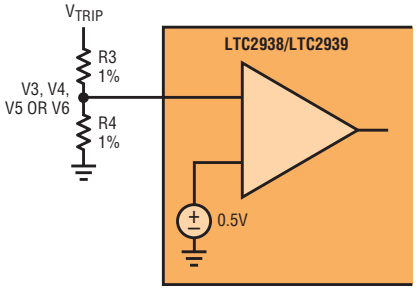


Figure 3. Setting the positive adjustable trip point, $V_{TRIP} = 0.5V \bullet (1 + R3/R4)$

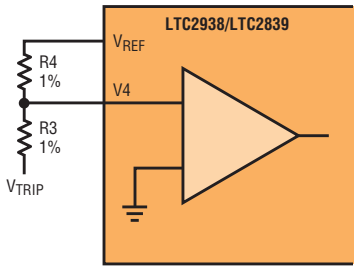


Figure 4. Setting the negative adjustable trip point, $V_{TRIP} = -V_{REF} \bullet (R3/R4)$

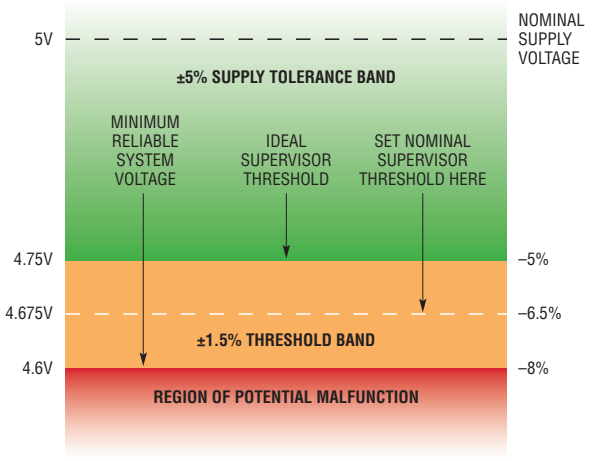


Figure 5. Tight 1.5% threshold accuracy improves system reliability

BUILT-IN GLITCH IMMUNITY

Monitored supply voltages are not perfectly flat DC signals but are contaminated by high frequency components caused by a number of sources such as the output ripple of the power supply or coupling from other signals. If the monitored voltage is near or at the reset threshold voltage, this noise could cause spurious resets. Fortunately, the LTC2938 and LTC2939 have been designed to deal with this potential issue, so spurious noise is of little to no concern.

Some supply monitors overcome spurious noise by adding hysteresis to the input comparator but this degrades monitor accuracy because the true accuracy of the trip threshold is now the percentage of added hysteresis plus the advertised accuracy of the part. The LTC2938 and LTC2939 do not use hysteresis, but instead use an integration scheme that requires transients to possess enough magnitude and duration to switch the comparators. This suppresses spurious resets without degrading the monitor accuracy. Figure 6 shows the response time of the input comparator versus input overdrive.

ADDITIONAL GLITCH FILTERING

Although all the comparators monitoring the supplies have built-in glitch filtering, additional bypass capacitors should be added to V1 and V2 as the higher of these voltages supplies the V_{CC} for the entire chip. Bypass capacitors may also be added to the V3, V4, V5 and V6 inputs to suppress troublesome noise on these supplies.

ADJUSTABLE RESET TIMEOUT PERIOD

The reset timer determines the minimum time duration (t_{RST}) that the $\overline{RST}$ output pulls low to reset the microprocessor and its peripheral circuits (see Figure 7). These are reset whenever any of the monitored supplies falls below its voltage threshold long enough to defeat the glitch filters or a watchdog timeout occurs. Once all the supplies are back above their respective threshold voltages again, the reset timer is started. $\overline{RST}$ remains low for t_{RST} seconds before $\overline{RST}$ is pulled back high, taking the microprocessor and the peripheral circuits out of reset.

To suit a variety of microprocessor applications, t_{RST} can be adjusted by connecting a capacitor (C_{RT}) between the CRT pin and ground. t_{RST} is chosen to allow the power supplies to settle down and ensure proper system reset. The value of this capacitor can be calculated from:

$$C_{RT} = \frac{t_{RST}}{2M} = 500\ \frac{pF}{ms} \bullet t_{RST}$$

This capacitor is charged by a nominal charging current of 2µA. The accuracy of the timeout period can be affected by capacitor leakage, so low leakage ceramic capacitors are recommended for C_{RT}. Leaving the CRT pin open generates a minimum reset period of approximately 20µs, a number that is highly sensitive to PCB stray capacitances.

OPEN-DRAIN RESET OUTPUT

The $\overline{RST}$ output of the LTC2938 and LTC2939 is an open-drain output and is internally pulled up to V2 by a weak current source (6µA). $\overline{RST}$ can be pulled to voltages higher than V2 by an external pull-up resistor. Multiple devices operating from different I/O voltages can be connected in a wired-OR configuration where the open-drain outputs are all tied together. This allows more than six supplies to be monitored with the same $\overline{RST}$ line. The open-drain output also permits $\overline{RST}$ to drive I/O circuits operating from different supply voltages and to reset these circuits at the same time as the microprocessor for a clean system restart. $\overline{RST}$ is guaranteed to be in the low state for V_{CC} > 1V ensuring reliable reset of the microprocessor until all the supplies have reached safe levels regardless of supply turn-on characteristics.

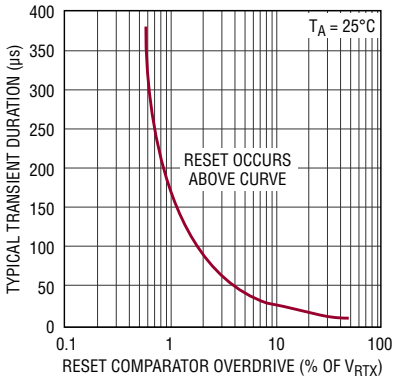


Figure 6. Transient duration versus comparator overdrive

WATCHDOG TIMER

The watchdog timer provides a means for a system to recover from software malfunctions or errors. For example, systems can fail when cosmic radiation corrupts registers or memory in today's microprocessors built with ultrafine geometries. A well designed watchdog timer is crucial for recovery from such conditions. The LTC2938 and LTC2939 watchdog timer works independently of the microprocessor and starts working on power-up once all the supplies are valid.

The watchdog timer starts whenever $\overline{RST}$ goes from low to high. The system software must clear the watchdog timer periodically to prevent it from timing out and resetting the microprocessor. This is done by flipping the state of the watchdog input (WDI) before the end of the watchdog timeout period (t_{WD}). Failing this, the watchdog times out and the watchdog output ($\overline{WDO}$) is latched low, which in turn causes $\overline{RST}$ to be pulled low, for a reset timeout period (t_{RST}), to reset the microprocessor. Once the reset timeout period has expired, the latched state of the watchdog output ($\overline{WDO}$) is cleared when transitions on the watchdog input (WDI) resume.

Before flipping WDI, the microprocessor may check the system to make sure that it is working properly, for it is possible for the code that kicks the watchdog to remain alive while the rest of the system has malfunctioned. If the system checks fail, then letting the watchdog timeout intentionally causes the system to reset completely for a proper recovery.

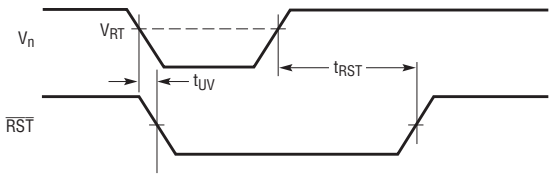
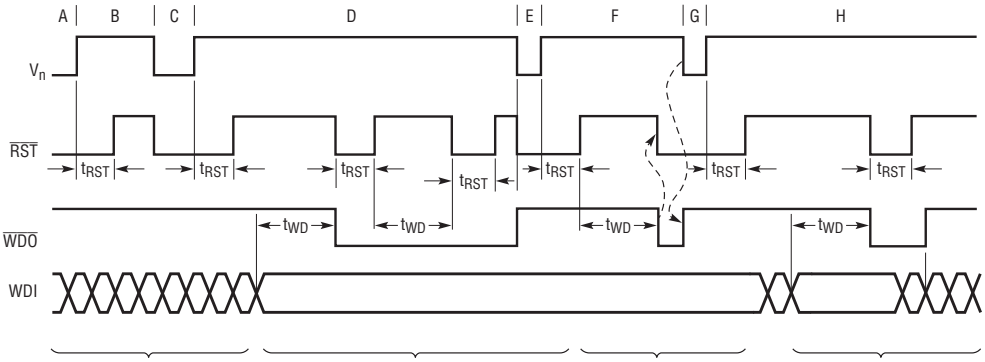


Figure 7. Reset timing

The WDI pin is a 3-state input. If this pin is left unconnected or tied to a high impedance node or if it is driven from a logic high or low state to a high impedance state, the watchdog timer is disabled and the C_{WT} capacitor is discharged to ground but $\overline{WDO}$ is not cleared. When left disconnected, a weak internal buffer drives the WDI pin to about 0.9V to detect a high impedance condition. This pin sinks or sources 10µA or less within the 0.7V to 1.1V range that defines the high impedance point. While WDI is high or low, it can sink or source up to 30µA. Another way to disable the watchdog is to simply short CWT to ground as this prevents timer operation. Disabling the watchdog is useful in systems that require the low supply monitoring capability of the LTC2838/39 but not the watchdog function.

Forcing or tying WDI either high or low enables the watchdog timer. WDI must transition between its V_{IL} and V_{IH} logic levels to either reset the timer to prevent timeout and discharge the C_{WT} capacitor

Figure 8. Watchdog and reset timing



The LTC2938 and LTC2939 are specifically designed to allow a microprocessor to distinguish between resets caused by input supply undervoltage or those due to software malfunction (watchdog timeout).

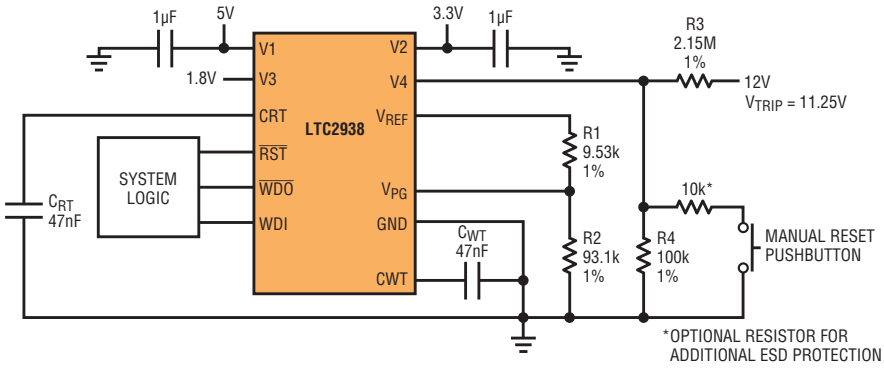


Figure 9. Quad-supply monitor (mode 14) with pushbutton reset

to ground or to clear the watchdog timer output ($\overline{WDO}$). Alternatively, if the WDI pin is pulsed between its low and high states to clear the watchdog timer, the pulse width must be at least 2µs. If WDI is driven from a high impedance state to a high or low logic state, $\overline{WDO}$ is not reset but the watchdog timer starts to run. This preserves the state of WDO when the microprocessor resets and takes its I/O pins out of high impedance. While $\overline{RST}$ is low, transitions on the WDI pin are ignored so that $\overline{WDO}$ remains latched for at least one reset period (t_{RST}).

OPEN-DRAIN WATCHDOG OUTPUT

The output of the watchdog timer or $\overline{WDO}$ is an open-drain output with a weak pull-up (6µA) to V2. Like $\overline{RST}$, it may be pulled to a higher supply voltage via an external pull-up resistor or connected in a wired-OR fashion to other watchdog outputs. $\overline{WDO}$ and $\overline{RST}$ should not be connected together since the first watchdog timeout will force $\overline{RST}$ low, which resets the microprocessor, making it impossible to toggle WDI to clear $\overline{WDO}$.

ADJUSTABLE WATCHDOG TIMEOUT PERIOD FOR SOFTWARE OPTIMIZATION

The LTC2938 and LTC2939 watchdog timeout period can be adjusted for optimal software performance. A capacitor connected from the CWT pin to ground sets the watchdog time out period. The value of the capacitor is determined from:

$$C_{WT} = \frac{t_{WD}}{20M} = 50\ \frac{pF}{ms} \bullet t_{WD}$$

Leaving CWT unconnected generates a minimum watchdog timeout of approximate 200µs. The maximum timeout period is limited by the largest available low leakage capacitor. Since the charging current is only about 2µA, low leakage ceramic capacitors are also recommended for C_{WT}. The value of C_{WT} takes into account the software overhead of having to hit the WDI pin periodically and how quickly the system needs to recover from a malfunction.

RESET AND WATCHDOG TIMING

The timing diagram in Figure 8 shows the relationship between the reset and watchdog timers. V_n represents any of the monitored supplies and a low state means an undervoltage (UV) condition. During a UV condition, $\overline{RST}$ and $\overline{WDO}$ are forced low and high respectively. In addition, the reset and watchdog timers are disabled and the C_{RT} and C_{WT} capacitors are discharged to ground. $\overline{RST}$ low (see time intervals A, C, E, and G) resets the microprocessor.

Once the undervoltage condition clears (V_n high), the reset timer is enabled. $\overline{RST}$ and $\overline{WDO}$ remain low and high respectively until the end of t_{RST} when $\overline{RST}$ is pulled high to take the microprocessor out of reset allowing it to start running the system software. This is seen during time intervals B, D, F and H. Once out of reset, the watchdog timer starts to run. During normal operation, the microprocessor toggles the WDI pin periodically to prevent watchdog timeout.

The LTC2938 (4-supply) is available in a 12-pin MSOP package while the LTC2939 (6-supply) is available in 16-pin MSOP and DFN packages.

However, if the software malfunctions and stops toggling WDI, the watchdog timer times out and latches $\overline{WDO}$ to a low state (e.g. interval D) and remains low until an undervoltage event occurs or WDI is toggled. Upon watchdog timeout, $\overline{RST}$ is also pulled low, resetting the microprocessor for t_{RST} seconds. It is then pulled high, allowing the microprocessor to restart the software from the beginning and recover from the malfunction. While the reset timer is running ($\overline{RST}$ low), toggling WDI does not clear $\overline{WDO}$ from a low state as seen at the extreme right of Figure 8. On exiting reset, the microprocessor examines the state of $\overline{WDO}$ to determine if the reset is caused by an undervoltage condition, which resets $\overline{WDO}$ to a high state; or by a watchdog timeout as indicated by a low $\overline{WDO}$ state. After $\overline{RST}$ is released, any transition between logic low and logic high at WDI clears $\overline{WDO}$. Therefore, the WDI pin should not be toggled until $\overline{WDO}$ state has been checked by the microprocessor. Some microprocessors place their I/O pins in high impedance during reset. Putting WDI in high impedance disables the watchdog timer and discharges C_{WT} to ground but does not affect the state of $\overline{WDO}$. If the microprocessor does not clear $\overline{WDO}$ and it remains in its latched low state, the reset and watchdog timers will run alternately and $\overline{RST}$ is pulled low each time the reset timer runs, thus repeatedly resetting the microprocessor. This can be useful in systems where $\overline{RST}$ is used to drive an interrupt rather than to reset the system, and the interrupt service routine hangs or is flawed.

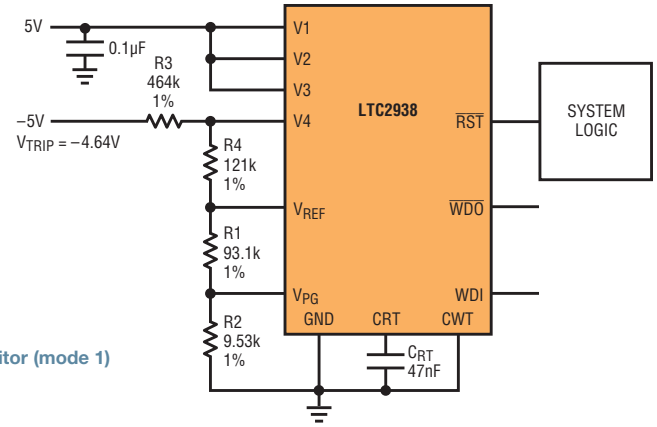


Figure 10. A ±5V supply monitor (mode 1) with unused inputs disabled

APPLICATIONS

Figure 9 shows a quad supply monitor with pushbutton reset. R1 and R2 are chosen to select mode 14 (see Table 1). In this mode, the V1, V2 and V3 inputs of the LTC2938 monitor 5V, 3.3V and 1.8V respectively while the V4 input, which is an adjustable input, is configured by resistors R3 and R4 to monitor a 12V supply with a trip point of 11.25V. The pushbutton function is simply implemented by shorting out the R4 resistor so that the V4 input registers an undervoltage condition, causing the LTC2938 to reset.

Figure 10 shows a circuit that monitors a split supply of ±5V. In this application, the LTC2938 is configured in mode 1 in which V1 monitors 5V and V4 becomes an adjustable pin that monitors negative voltages. R3 and R4 configure V4 to monitor –5V with a threshold of –4.64V. In this application, the CWT pin is tied to ground to disable the watchdog circuit. The V2 and V3 inputs are unused and are tied to V1 to prevent the V2 and V3 comparators from affecting the $\overline{RST}$ Output.

CONCLUSION

The LTC2938 and LTC2939 are specifically designed to allow a microprocessor to determine whether a system reset is due to undervoltage or to software malfunction (watchdog timeout). They can monitor four or six supplies respectively and come in small DFN or MSOP packages to save valuable board space. The LTC2938 is available in a 12-pin MSOP package while the LTC2939 is available in 16-pin MSOP and DFN packages. Both include single-pin selection of one of 16 possible supply threshold configurations. Thresholds are accurate to ±1.5%, which simplifies system design by narrowing the voltage range in which the system must operate. Commercial, industrial and automotive temperature grades are all available. Comparator glitch immunity prevents false resets and adjustable reset and watchdog timeout periods allow customization to the hardware and software requirements of individual systems. ■

Accurate Constant-Current, Constant-Voltage 20A Power Supply Ensures Safe Charging of Supercaps and Li-Ion Batteries

Josh Caldwell

Many applications require a power supply that can accurately regulate a voltage *and* accurately limit output current, but there are remarkably few solutions that can do both with a single IC. System designers must typically trade off accuracy in one feature for accuracy in the other by choosing between a high gain, high accuracy voltage regulator with a crude current limit or a high accuracy current regulator with a crude voltage clamp.

The LT®3741 simplifies the design of constant-current, constant-voltage regulators by combining an accurate current regulator and an accurate voltage regulator in a single IC, thus eliminating power system design trade-offs. The LT3741 is a synchronous buck DC/DC controller designed to regulate output currents up to 20A and output voltages up to 34V, with a current regulation accuracy of ±6% and a voltage accuracy of ±1.5%. Near-ideal constant voltage and constant current regulation is possible because of the LT3741's average current mode control architecture. As seen in Figure 1, the transition between the voltage and current loop is seamless and extremely sharp.

A unique topology allows the LT3741 to both sink and source current. Precise load current control is achieved with analog control pins CTRL1 and CTRL2. The switching frequency can be programmed from 200kHz to 1MHz and synchronized to an external clock from 300kHz to 1MHz.

SINGLE-CELL LITHIUM-ION BATTERY CHARGER PROVIDES 10A OF CHARGING CURRENT

Safety concerns and thermal limitations of charging lithium-ion batteries mean the charger must be able to carefully control charging currents and voltages. Ideally, a microcontroller can accurately throttle back the charging current during the initial and top-off charging phases. This forces the use of a current regulation scheme that has precision adjustable current control, thermal limiting capabilities, and an accurate voltage limit.

The LT3741 easily meets these requirements. Figure 2 shows the LT3741 configured as a lithium-ion battery charger with the maximum current limit set at 10A and the voltage limit set at 4.2V. Charging current is independent of the output voltage and can be adjusted down to 0A via CTRL1. The voltage divider from V_{REF} to

Figure 1. V_{OUT} vs I_{OUT} for a 200W, 10V/20A constant-current, constant-voltage step-down converter

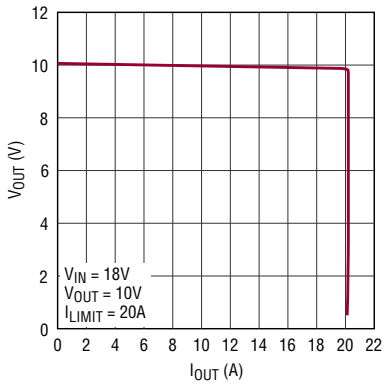
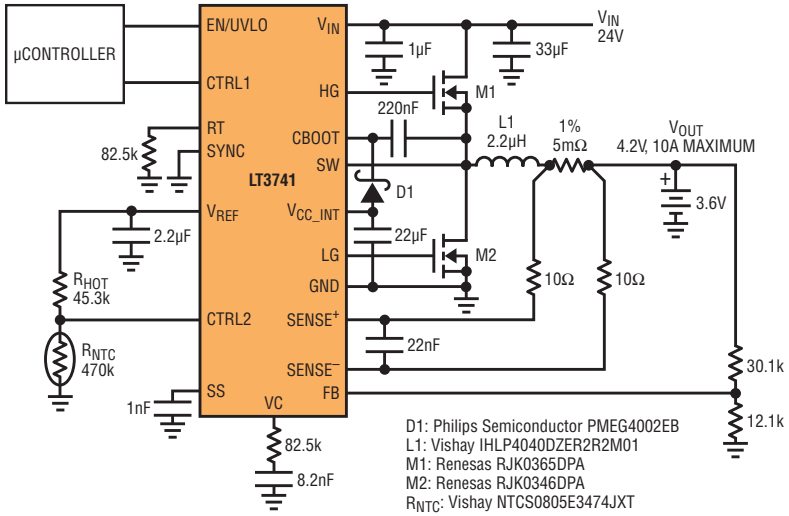


Figure 2. A 10A single-cell lithium-ion battery charger



CTRL2 provides the thermal limit control using a temperature dependent resistor.

With the sharp transition between current and voltage control, the LT3741 delivers system reliability and safety by allowing the battery to be charged with constant current up to the voltage regulation point. Efficiency for this solution is about 93%.

THERMALLY DERATING THE LOAD CURRENT

Proper thermal management is essential with any high power regulator to both protect the load and reduce the chance of system-wide damage. The LT3741 uses the CTRL2 pin to reduce the regulated inductor current. Whenever CTRL2 is lower than the analog control voltage on the CTRL1 pin, the regulated current is reduced. The temperature derating is programmed using a temperature dependent resistor divider from the V_{REF} pin to ground.

SUPERCAPACITOR CHARGER

Supercapacitors are replacing lead-acid batteries in a number of applications from rapid-charge power cells for cordless tools to short-term backup power for microprocessors to vehicle and mobile defense applications. Although each of these applications reaps different benefits from using a supercapacitor, they all require careful control of the charging current and voltage limiting to prevent system-wide damage or damage to the supercapacitor. The charging power source must provide an accurately regulated current source to the supercapacitor, regardless of output voltage while providing an accurate voltage limit to prevent overcharging.

Figure 3 shows a 20A supercapacitor charger with a 5V regulated output voltage. Utilizing a wide input-common-mode range error amplifier for current regulation, the LT3741 provides accurate charging currents through a broad-range of output voltages including a short on the output. This is essential to prevent excessive heat dissipation and limit the charging current within a completely discharged supercapacitor. In Figure 4, the output voltage is plotted verses output current for this charger, showing the LT3741 maintaining current regulation into a virtually shorted output.

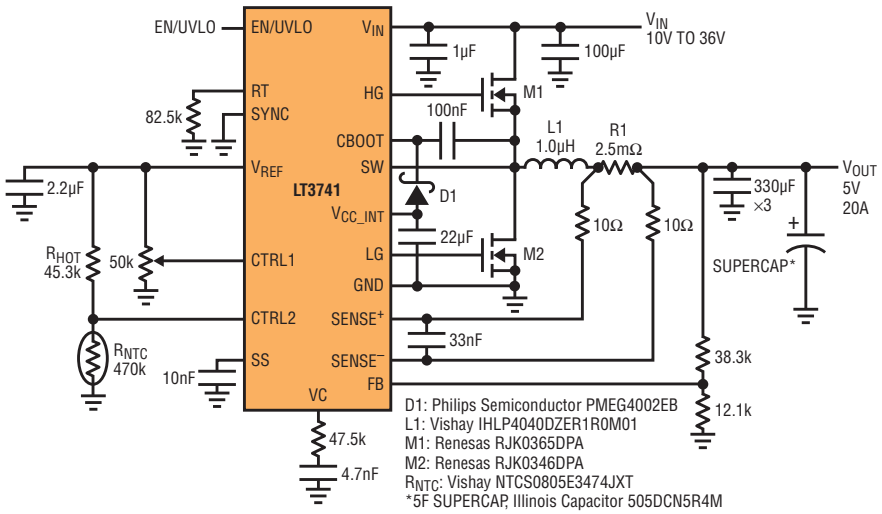


Figure 3. A 20A supercapacitor charger with 5V regulated output

STRONG GATE DRIVERS AND HIGH CURRENT LDO

Modern high current switching Power MOSFETs are most efficient when driven with low resistance drivers to reduce transitional losses. The LT3741 contains very strong gate drivers. The LG and HG PMOS pull-up driver on-resistance is typically 2.3Ω. The on-resistance of the LG and HG NMOS pull-down drivers are typically less than 1.3Ω. While the gate drivers reduce losses, the LT3741 is also capable of driving two high current MOSFETs in parallel where load currents exceed 20A. The LT3741 utilizes a 5V internal high current low dropout voltage regulator to provide up to 50mA to the gate drivers.

Figure 4. Output voltage vs load current for a 5V/20A supercapacitor charger

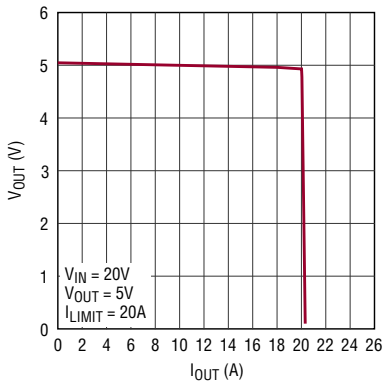
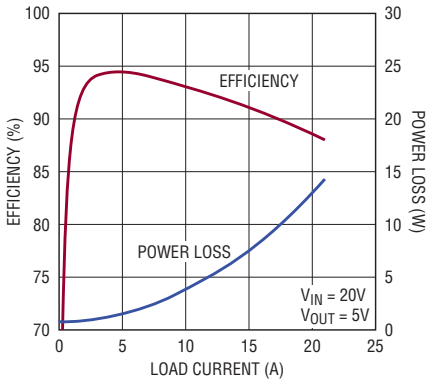


Figure 5. Efficiency and power loss vs load current for the 20A supercapacitor charger



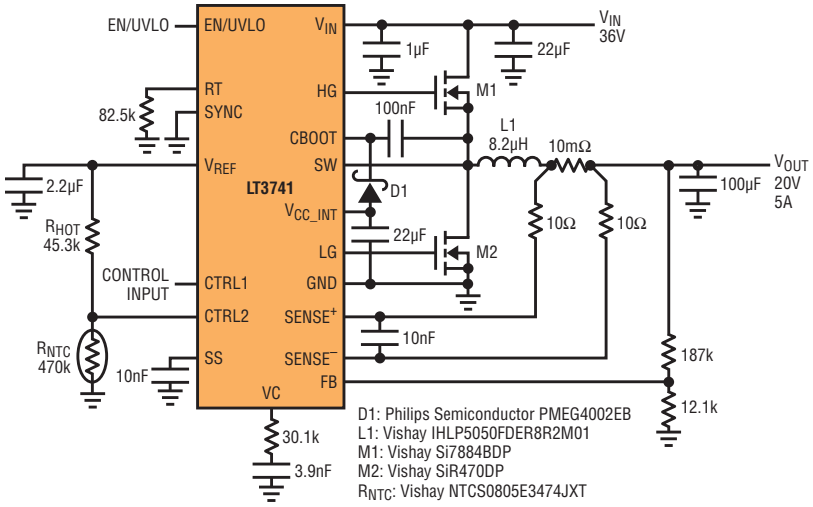


Figure 6. A 100W 20V/5A constant-current, constant-voltage step-down converter

A 100W 20V/5A CONSTANT-CURRENT/CONSTANT-VOLTAGE STEP-DOWN CONVERTER

The LT3741 may be used as a general-purpose power solution where accurate output current limit is required. Figure 6 shows a 500kHz, 100W, 20V/5A constant-current, constant-voltage converter. Average current mode control keeps the LT3741 stable and allows it to readily to meet any output voltage or current requirements. For additional protection, the LT3741 utilizes a common mode lock-out circuit that prevents the output from exceeding the input common mode range of the current control loop error amplifier.

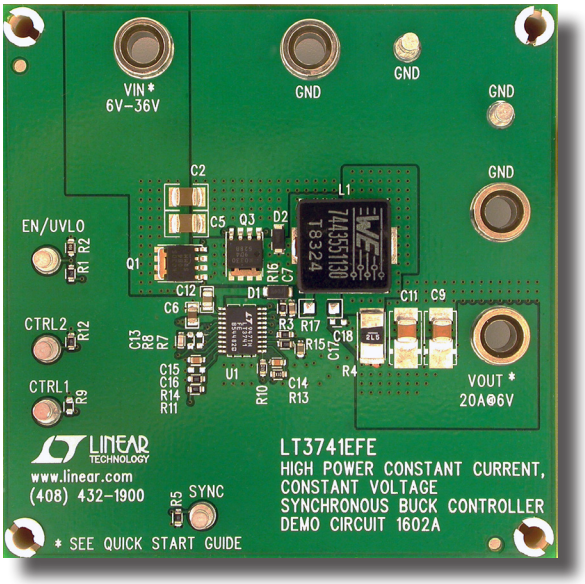
COMPACT SOLUTION

The LT3741 is available in a 20-pin exposed pad TSSOP or 20-pin 4mm × 4mm exposed pad QFN, creating a complete, uncompromising power solution that can takes up a mere 1.5in². The part is designed specifically for use with low inductance, high saturation current inductors, further reducing board area and profile height. Figure 7 shows a demonstration circuit that produces a 6V/20A constant-current, constant-voltage output. The components in this particular design have standard footprints, making it easy to switch them out to adjust the output current limit and regulated voltage.

CONCLUSION

The LT3741 offers accurate current and voltage regulation for constant-current and constant-voltage applications with nearly ideal voltage and current regulation characteristics. The combination of a high gain current control-loop and an equally high gain voltage control loop relaxes the tolerance requirements of other power supply components, thus reducing overall cost, complexity and board size. Average current mode control allows the use of low value, low cost, high saturation current inductors to further reduce overall board footprint. With the demands of today's battery and supercapacitor chargers, and system requirements for high accuracy current limit and voltage regulation, the LT3741 provides a versatile power solution. ■

Figure 7. DC1602A high power constant-current, constant-voltage demo circuit



4mm × 7mm IC Produces Seven Regulated Outputs and a Dual-String LED Driver

Aspiyan Gazder

The LTC3675 is a space-saving single-chip power solution for multirail applications that run from a single Li-ion cell. Its 4mm × 7mm QFN contains two 500mA buck regulators, two 1A buck regulators, a 1A boost regulator, a 1A buck-boost regulator, a boost LED driver capable of driving dual LED strings up to 25mA, and an always-on 25mA LDO for powering a housekeeping microprocessor. All regulators can be controlled via I²C. Figure 1 shows an eight-rail solution run from a single Li-ion battery.

SWITCHING REGULATOR FEATURES

All of the voltage regulators in the LTC3675 are internally compensated monolithic synchronous regulators. The buck regulators and the buck-boost regulator can be enabled via enable pins or I²C, whereas the boost regulator is enabled via I²C only. The feedback regulation voltage of the regulators can be programmed via I²C from 425mV to 800mV in 25mV steps.

Each regulator offers two modes of light load operation. The buck regulators offer Burst Mode operation for the greatest efficiency and pulse skipping-mode for more predictable EMI. The boost and buck-boost regulators offer Burst Mode operation and PWM mode. Each regulator's operating mode can be programmed via I²C.

The regulators also feature I²C-programmable slew rate control on the switch edges, where fast switching produces higher efficiency and slow switching improves EMI performance.

PARALLEL BUCK REGULATORS FOR INCREASED LOAD CURRENT CAPABILITY

Any two successively numbered buck regulators of the LTC3675 can be combined in parallel to produce a single regulator output with a combined load current capability. For instance, buck regulators 1 (capable of 1A) and 2 (capable of 1A) can be paralleled to produce a single buck regulator capable of delivering up to 2A of load current. Similarly, buck regulators 2 and 3 can be paralleled to make a single buck regulator with load capability up to 1.5A and buck regulators 3 and 4 can be paralleled to make a single buck regulator with load capability up to 1A.

When two buck regulators are combined, the lower numbered buck regulator serves as the master and controls the power stage of the higher numbered slave buck regulator. The behavior of the combo buck regulator is programmed via the master (lower numbered) regulator. To configure a buck regulator as a slave, its feedback pin must be connected to V_{IN} and the switch nodes of the master and slave buck regulators are shorted together to a common inductor. The trace impedances of both master and slave must be kept the same from the switch pins to the inductor to obtain better current flow distribution in the two power stages. Unequal trace impedance may compromise on the load capability of the combo buck regulator.

Figure 2 shows an application in which buck regulators 1 and 2 have been paralleled with buck regulator 1 as the master and buck regulator 2 as the slave.

LED DRIVER FEATURES

The LED driver is capable of driving two LED strings with up to 10 LEDs each. The LED driver may alternately be configured as a high voltage boost regulator.

When configured as a dual string LED driver, the lower of the voltages at the LED1 or LED2 pins is the regulation point. In Figure 1, the 20k resistor at the LED_FS pin programs the LED full-scale current to 25mA. Better than 1% matching between the two LED strings is achieved at this current level. An automatic gradation circuit allows the LED current to change levels at a rate programmed by the user.

For applications that require LEDs to be biased at currents higher than 25mA, the programmed current can be doubled by setting a bit in the program register via I²C. For a LED_FS resistor of 20k, setting this bit programs a full-scale current of 50mA. When used in this mode the output voltage is limited to 20V.

LED DRIVER CONFIGURED AS A HIGH VOLTAGE BOOST REGULATOR

The LED driver can be configured to operate as a high voltage boost regulator using an I²C command. The LED_OV pin acts as the feedback pin. An output voltage up to 40V can be programmed using external resistors. In Figure 2 the LED driver

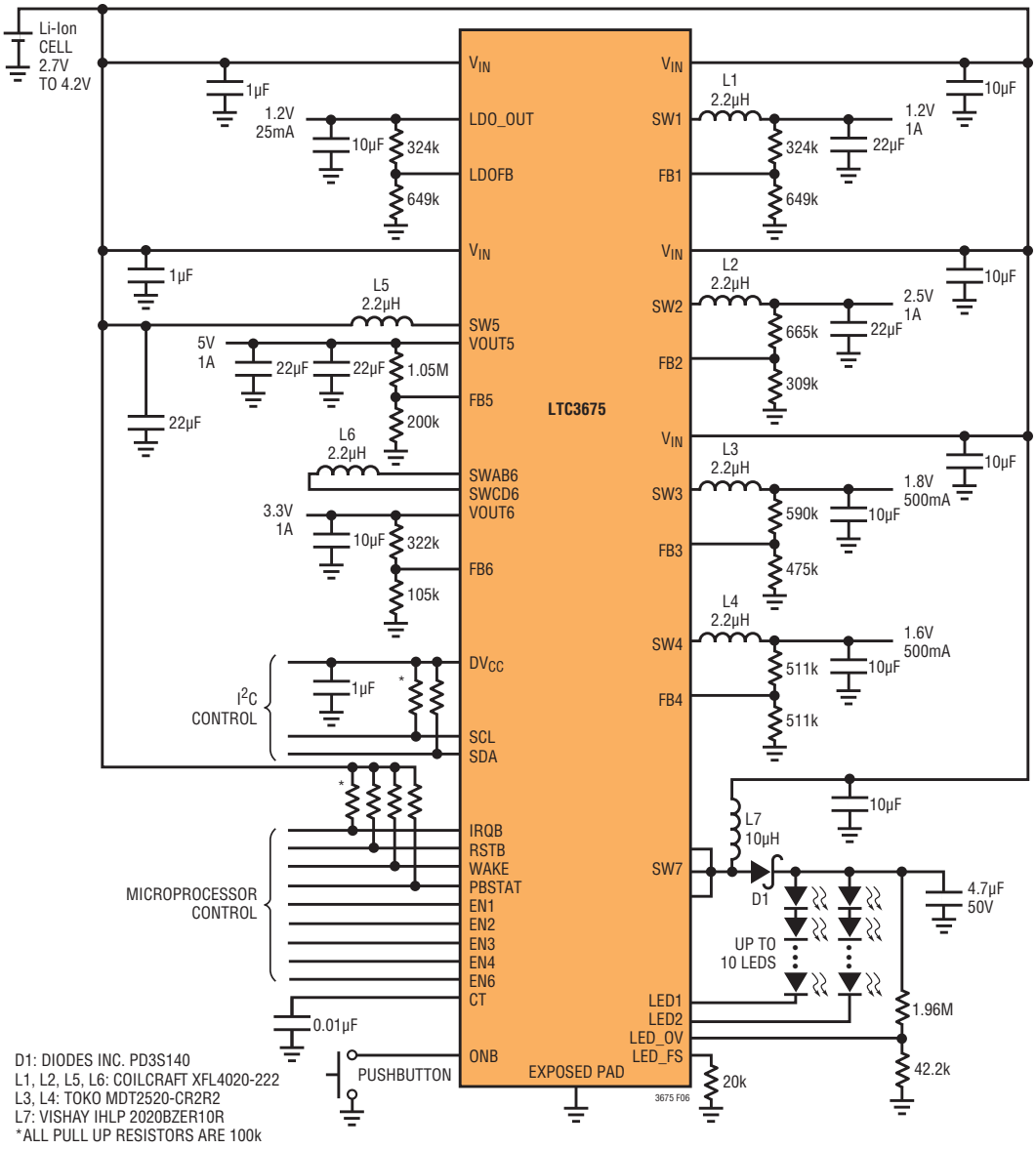


Figure 1. Li-ion cell to eight power rails, including an LED driver, using a single IC

is configured as a boost regulator that provides a 12V output. To maintain stability, the average inductor current must not exceed 750mA. For a 12V output, up to 150mA of load current can be supplied over the entire input voltage range.

PUSHBUTTON INTERFACE AND SEQUENTIAL POWER UP

The LTC3675 can be powered up or powered down using the ONB pin. All timing related to the ONB, RSTB and WAKE pins are programmed by the CT capacitor. In the discussion below, a CT capacitor of 0.01µF is assumed.

Regulators may be started up sequentially using the pushbutton interface and precision enable thresholds. When all regulators are off, the enable pin threshold is 650mV. Once a regulator has been enabled either via I²C or its enable pin, the thresholds of the remaining enable pins is set to precisely 400mV. This allows a well controlled sequential power up.

After initial power up and if no regulator has yet been enabled, holding the ONB pin low for 400ms causes the WAKE pin to go high for five seconds. The WAKE pin may be hard tied to an enable pin to power up any individual regulator, whose output may then be used to power up another regulator. In this fashion, the LTC3675 can be sequentially powered up as shown in Figure 3. Figure 4 shows the sequential power up of buck regulator 1 followed by buck regulator 2 and then by buck regulator 3. Before the WAKE pin goes LOW, an I²C command must be written to reinforce the enabled status of buck 1. Otherwise, when WAKE is pulled low, buck regulator 1 shuts off, causing buck regulators 2 and 3 to power down as well.

If the LTC3675 has one or more regulators enabled, pressing the ONB pin for five seconds generates a hard reset. A

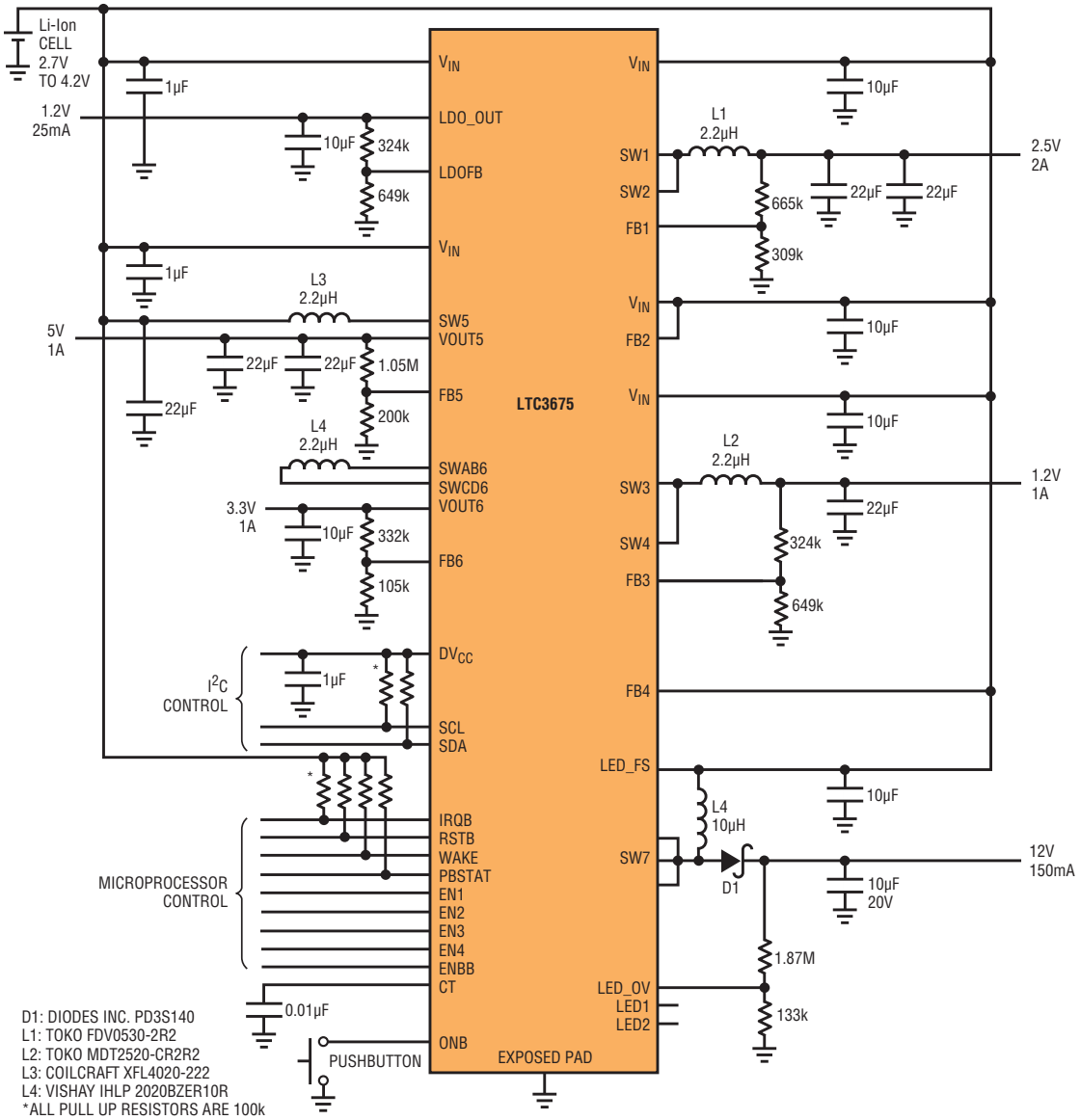


Figure 2. Paralleling buck regulators 1 and 2 ups the load current capability. The 12V output is produced using the boost typically used for LED strings.

hard reset causes all enabled regulators to power down for one second. After one second, the hard reset state is exited and the I²C registers are all set to their default state. A hard reset may also be generated using the RESET_ALL bit via I²C command.

The PBSTAT pin reflects the status of the ONB pin once the LTC3675 is in the ON state. At initial power up, if the ONB pin is pulled low and all regulators are off, PBSTAT remains in the high impedance state. If a regulator is enabled, ONB going low for at least 50 ms will cause PBSTAT to also go low.

I²C FEATURES

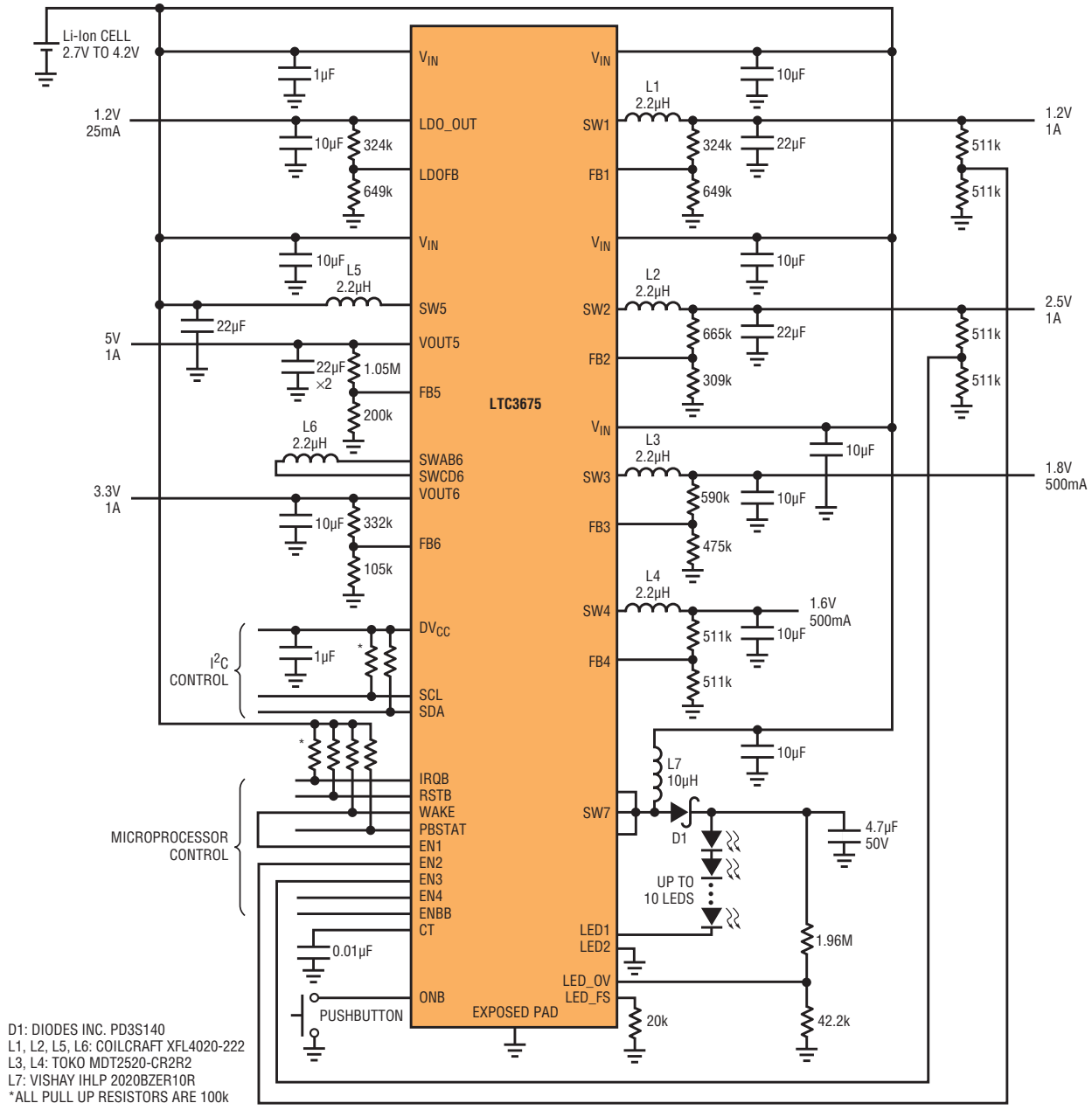
The I²C interface provides both programmability and status reporting via 11 program registers and 2 status registers. The contents of these registers can be read at any time to ensure proper operation.

Each switching regulator is associated with a single program register while the LED driver is controlled by two program registers. The UVOT program register is used to select one of eight preset undervoltage warning thresholds and one of three preset die temperature warning thresholds.

The I²C port is also used to reset the IRQB pin and the latched status register bits in the event that a fault has occurred.

ERROR CONDITION REPORTING—USING RSTB AS A POWER ON RESET

The LTC3675's RSTB and IRQB pins are pulled low when reporting an error condition—otherwise they remain in a high impedance state. Reported error conditions include out-of-regulation



D1: DIODES INC. PD3S140
L1, L2, L5, L6: COILCRAFT XFL4020-222
L3, L4: TOKO MDT2520-CR2R2
L7: VISHAY IHLP 2020BZER10R
*ALL PULL UP RESISTORS ARE 100k

Figure 3. Single string LED driver with regulator start-up sequencing

output voltages, input undervoltage and overtemperature warnings.

Each voltage regulator has an internal power good (PGOOD) signal that indicates the status of its output voltage. The output voltage of a regulator is defined as bad if it is enabled and the output voltage is below its programmed value by more than 7.5%. The PGOOD bit is set to zero indicating the output voltage is bad. The LED driver PGOOD signal is used only when it is configured as a high voltage boost regulator.

A PGOOD bit going low will pull RSTB low if unmasked. When the error condition is cleared, the RSTB pin goes back to its high impedance state. The user can selectively mask out an error condition from pulling RSTB low by programming the RSTB mask register. As an example, if the boost regulator is enabled but the user does not need to know the status of its output, the user can program the RSTB mask register such that a bad output at the boost regulator will not cause RSTB to be pulled low.

The RSTB pin may be used to implement a power on reset function. After a regulator has been enabled, the RSTB pin is pulled low and stays low until the output voltage has been above its PGOOD threshold for 200ms. After that, the RSTB pin returns to its high impedance state. The above example assumes that the RSTB mask register contents are such that the PGOOD signal of the enabled regulator is allowed to pull the RSTB pin low.

The LTC3675 is ideally suited for applications that require multiple power rails from a single Li-ion battery source. Six regulators combined with a dual string LED driver set the LTC3675 apart from competing power management solutions.

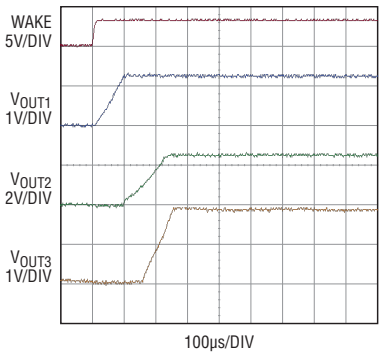


Figure 4. Sequenced start-up of the four buck regulators

The IRQB pin is also pulled low when an error is generated and stays low even if the error condition has been corrected. The IRQB pin is cleared using an I²C command. In addition to reporting a bad regulator output voltage, the IRQB is also pulled low if either the input undervoltage or overtemperature warning thresholds have been exceeded. By programming the IRQB mask register, it is possible to selectively mask the error conditions that cause IRQB to be pulled low. The input undervoltage warning and overtemperature warning conditions cannot be masked.

The data in the real time status and latched status registers reveal the exact nature of the fault. The condition of the error reporting bits in the real time status register changes as the error conditions change. The latched status register information is latched when an unmasked error condition occurs—the contents of the register do not change after the latching event. The contents of the latched status register are cleared during an IRQB clear command.

INPUT UNDERVOLTAGE FAULT WARNING AND SHUTDOWN

The LTC3675 is capable of operating at input voltages down to 2.7V. Nevertheless, other devices may need to shut down or enter a low power state before the Li-ion discharges all the way to 2.7V. The LTC3675 includes an input undervoltage warning signal, with a threshold set to one of eight levels via I²C. When the input voltage drops to the programmed threshold voltage, the IRQB pin is pulled low, indicating a fault. The status register can be read to determine the fault and take any corrective action needed.

The LTC3675 also includes an input undervoltage shutdown, which turns off all enabled regulators if the input supply voltage drops below 2.45V. The contents of the program registers are reset to their default state. Operation resumes once the input voltage increases above 2.55V.

OVERTEMPERATURE FAULT WARNING AND SHUTDOWN

The LTC3675 is capable of delivering more than 15W of output power in a very small amount of board space. Even with its high efficiency regulators, the combined efficiency losses produce dissipated heat, which raise the die temperature. To protect the die and other components, the LTC3675 includes four I²C-selectable die temperature warning thresholds. When the die temperature exceeds the selected warning threshold, the IRQB pin pulls low. In the event of a warning, the status register can be read to determine the fault.

If the die temperature exceeds 150°C, all enabled regulators are shut down and the program registers are reset to their default state. Operation resumes once the die temperature drops below 135°C.

CONCLUSION

The LTC3675 is ideally suited for applications that require multiple power rails from a single Li-ion battery source. Six regulators combined with a dual string LED driver set the LTC3675 apart from competing power management solutions. I²C programmability and fault reporting give system designers the ability to maximize battery run time with efficient battery power usage and active thermal management. The LTC3675 is available in a space saving 4mm × 7mm QFN package. ■

Battery-Free Power Backup System Uses Supercapacitors to Prevent Data Loss in RAID Systems

Jim Drew

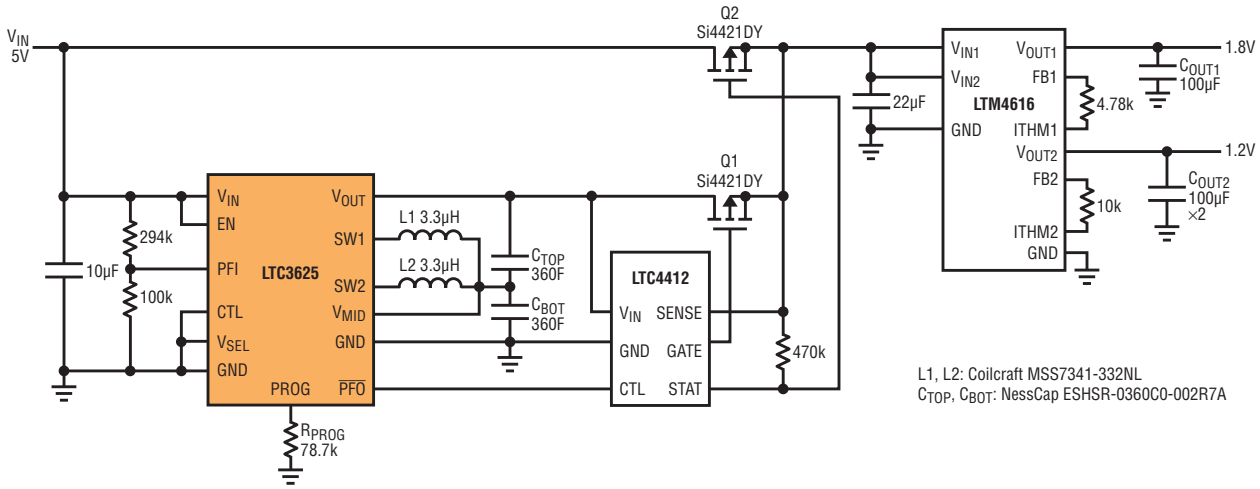
RAID systems by their very nature are designed to preserve data in the face of adverse circumstances. One such circumstance, a power failure, does not directly threaten data that is stored on disks, but it does compromise data in transit or data that is temporarily stored in volatile memory. To protect volatile data, many systems incorporate a battery-based power backup system that supplies short-term power—enough watt-seconds for the RAID controller to write volatile data to nonvolatile memory.

The problem is that increased performance demands and green initiatives are putting pressure on system designers to find alternatives to batteries. Batteries are a notoriously hazardous material that must be disposed of under the strict guidelines set by regulatory agencies. Because they require regular replacement whether used or not, battery replacement and disposal is a serious consideration in the cost of running a data center.

Advancements in flash memory performance have made it possible to replace the batteries in these systems with longer-lasting, higher performance and greener supercapacitors. Supercapacitors are made of carbon and aluminum and contain no heavy metals, so they do not present any hazardous material disposal issues. Also, supercapacitors are more robust than batteries, thus decreasing maintenance costs—the cycle life of Li-ion batteries is 500 cycles while a supercapacitor offers a cycle life of one million cycles. Supercapacitors can be recharged to full capacity in minutes where as batteries may take as long as six hours. Although the energy density of a supercapacitor may be as much as two orders of magnitude less than a Li-ion battery, reduced power requirements in flash memory and increased supercapacitor capacities have made them a viable energy storage medium for data-recovery backup solutions.

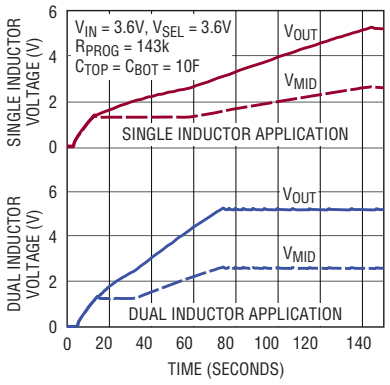
In a supercapacitor-based backup power system, a series connected capacitor stack must be charged and the cell voltages balanced. The supercapacitors are switched into the power path when needed and the power to the load is controlled by a DC/DC converter. Figure 1 shows a supercapacitor-based power backup system using an LTC3625 supercapacitor charger, an automatic power crossover switch using the LTC4412 and an LTM4616 dual output DC/DC converter.

Figure 1. Circuit implementation of a supercapacitor energy storage system for holding up power during a power fault.



Advancements in flash memory performance have made it possible to replace the batteries in power holdup systems with longer-lasting, higher performance and greener supercapacitors.

Figure 2. Charge profile into matched supercaps



The LTC3625 is a high efficiency supercapacitor charger that has a number of features that makes it an ideal choice for small profile backup in RAID applications. It comes in a 3mm × 4mm × 0.75mm 12-lead DFN package and requires few external parts. It features programmable average charge current up to 1A, automatic voltage cell balancing of two series-connected supercapacitors and a low quiescent current. When the input power is removed or the part is disabled, the LTC3625 automatically enters a low current state drawing less than 1µA from the supercapacitors.

SUPERCAPACITOR CHARACTERISTICS

Supercapacitors are available in capacitances that range from the hundreds of millifarads to thousands of farads. The standard voltage ratings are 2.5V and 2.7V, while packaged, stacked supercapacitors can be greater than 15V. A 10F/2.7V supercapacitor is available in a 10mm × 30mm 2-terminal radial can while a 400F/2.7V supercapacitor is in a 35mm × 62mm 4-terminal radial can. Two of the four terminals in the larger can are for mechanical stability and are not electrically connected to either power terminal.

The two critical parameters of the supercapacitor to a backup power application are the initial leakage current and the cell voltage. The initial leakage current may be as much as 50 times the rated leakage current and decreases to the specified current after 100 hours at rated voltage. The applied voltage across the supercapacitor has a significant effect on its operating life. When charging series connected supercapacitors, voltage balancing is a key requirement of the charging circuit to preserve capacitor life. Passive voltage balancing, where a resistor is placed in parallel with each supercapacitor, is a simple technique but one that continually discharges the supercapacitor when the charger is disabled. Active voltage balancing, such as that performed by the LTC3625 during the charging process, eliminates the need for these resistors and prevents overcharging of the supercapacitors.

BACKUP POWER APPLICATIONS

An effective power backup system incorporates a supercapacitor stack that has the capacity to support a complete data transfer out of volatile memory. A DC/DC converter takes the output of the supercapacitor stack and provides a constant voltage to the data recovery electronics. The data transfer must be completed before the voltage across the supercapacitor stack drops to the minimum input operating voltage (V_{UV}) of the DC/DC converter.

To estimate the minimum capacitance of the supercapacitor stack, the effective circuit resistance (R_T) needs to be determined. R_T is the sum of the ESR of the supercapacitors, the distribution losses (R_{DIST}) and the $R_{DS(ON)}$ of the automatic crossover's MOSFETs.

$$R_T = ESR + R_{DIST} + R_{DS(ON)}$$

Allowing 10% of the input power to be lost in the effective circuit resistance at the point when the voltage into the DC/DC converter is at V_{UV}, the maximum value of R_T may be determined by:

In a supercapacitor-based backup power system, a series connected capacitor stack must be charged and the cell voltages balanced. The supercapacitors are switched into the power path when needed and the power to the load is controlled by a DC/DC converter.

$$R_{T(MAX)} = \frac{0.1 \bullet V_{UV}^2}{P_{IN}}$$

The voltage required across the supercapacitor stack ($V_{C(UV)}$) at this minimum operating voltage of the DC/DC converter:

$$V_{C(UV)} = \frac{V_{UV}^2 + P_{IN} \bullet R_T}{V_{UV}}$$

The minimum capacitance (C_{MIN}) requirement can now be calculated based on the required backup time (T_{BU}) to transfer data into the flash memory, the initial stack voltage ($V_{C(0)}$) and ($V_{C(UV)}$).

$$C_{MIN} = \frac{2 \bullet P_{IN} \bullet T_{BU}}{V_{C(0)}^2 - V_{C(UV)}^2}$$

The minimum capacitance (C_{MIN}) is the effective capacitance (C_{EFF}) of the stack of supercapacitors, which is the capacitance of one supercapacitor divided by the number of supercapacitors in the stack. The ESR used in the expression for calculating R_T is the product of the ESR of one supercapacitor times the number of supercapacitors in the stack. The end of life of a supercapacitor is defined as when the capacitance drops to 70% of its initial value or the ESR doubles in value. This end of life definition is used in selecting the supercapacitor for the design.

Both the ESR and capacitance of the supercapacitor decrease as the applied frequency increases. Manufactures generally specify the ESR at 1kHz while some specify the ESR at 1kHz as well as at DC. The capacitance is usually specified at DC. One method of determining the actual capacitance and ESR of the supercapacitor is to apply a constant current (I) to a charged supercapacitor and use the voltage decay to determine these parameters. The initial step in voltage (ΔV_C), neglecting any inductance effect of the supercapacitor, is used to determine the ESR.

$$ESR = \frac{\Delta V_C}{I}$$

After the initial step in voltage, the voltage across the supercapacitor decreases linearly due to the constant current load. By measuring the voltage at two time intervals, the capacitance of the supercapacitor can be determined.

$V_{C(t1)}$ is the voltage at the first time interval (t1)

$V_{C(t2)}$ is the voltage at the second time interval (t2)

$$C = \frac{I \bullet (t2 - t1)}{V_{C(t1)} - V_{C(t2)}}$$

The final parameter to determine is the charging current (I_{CHARGE}) of the supercapacitors. The charging current is determined by the desired recovery time or recharge time ($T_{RECHARGE}$) of the stack of supercapacitors.

The charging profile of the supercapacitors using the LT3625 is not the classic linear voltage ramp that one would expect (see Figure 2). This is due to the buck-boost topology of the LT3625.

The bottom supercapacitor of a two-capacitor stack is charged first to approximately 1.35V ($V_{MID(GOOD)}$). Once the bottom capacitor reaches 1.35V the boost circuit starts to charge the top supercapacitor, removing charge from the bottom supercapacitor. The buck converter continues to charge the bottom supercapacitor but the rise in voltage is slower since some of its charge is being removed. If the boost converter's input current is greater than the buck converters output current, voltage on the bottom supercapacitor decreases, and when it decays by the $V_{MID(GOOD)}$ hysteresis, the boost converter turns off and remains off until the bottom supercapacitor charges back to $V_{MID(GOOD)}$.

If the top supercapacitor exceeds the bottom supercapacitor by 50mV, the boost converter turns off until the bottom supercapacitor is 50mV above the top supercapacitor. Finally if the bottom supercapacitor reaches its maximum threshold, the buck converter turns off and the boost converter remains on. The voltage on the bottom supercapacitor deceases and the buck converter remains off until the voltage decreases by 50mV. This process continues until V_{OUT} reaches its programmed charger termination voltage.

The graph in Figure 2 shows the charge profile for two configurations of the LTC3625 charging a stack of two 10F supercapacitors to 5.3V with R_{PROG} set to 143k. This graph, combined with the following equation, is used to determine the value of R_{PROG} that would produce the desired charge time for the actual supercapacitors in the target application.

$$R_{PROG} = 143k \bullet \frac{10F}{C_{ACTUAL}} \bullet \frac{5.3V - V_{C(UV)}}{V_{OUT} - V_{C(UV)}} \bullet \frac{T_{RECHARGE}}{T_{ESTIMATE}}$$

The LTC3625 is an efficient 1A supercapacitor charger with automatic cell balancing that can be combined with the LTC4412 low loss PowerPath controller to produce an energy storage system that protects data in RAID disk applications.

$V_{C(UV)}$ is the minimum voltage of the supercapacitors at which the DC/DC converter can produce the required output. V_{OUT} is the output voltage of the LTC3625 in the target application (set by V_{SEL} pin). $T_{ESTIMATE}$ is the time required to charge from $V_{C(UV)}$ to the 5.3V, as extrapolated from the charge profile curves. $T_{RECHARGE}$ is the desired the recharge time in the target application.

The initial charge time at start-up is determined from the full charging time of 70 seconds.

$$T_{STARTUP} = 70s \bullet \frac{V_{OUT}}{5.3V} \bullet \frac{C}{10F} \bullet \frac{R_{PROG}}{143k}$$

DESIGN EXAMPLE

For example, say it takes 45 seconds to store the data into flash memory where the input power to the DC/DC converter is 20W. V_{UV} of the DC/DC converter is 2.7V. A $T_{RECHARGE}$ of ten minutes is desired. The voltage applied to the supercapacitor directly affects its lifetime so we do not want to apply full rated voltage (2.7V) across each stacked cap. The full charge voltage of the stack is set to 4.8V—a good compromise between extending the life of the supercapacitor and utilizing as much of the storage capacity as possible. The components of R_T are estimated: $R_{DISTRIBUTION}$ = 10mΩ, ESR = 20mΩ and $R_{DS(ON)}$ = 10mΩ.

$$\begin{aligned} R_T &= R_{DIST} + ESR + R_{DS(ON)} \\ &= 2 \bullet 10m\Omega + 10m\Omega + 10m\Omega \\ &= 40m\Omega \end{aligned}$$

$$R_{T(MAX)} = \frac{0.1 \bullet (V_{UV})^2}{P_{IN}} = \frac{0.1 \bullet 2.7V^2}{20W} = 36.5m\Omega$$

The resulting estimated values of $R_{T(MAX)}$ = 36mΩ and R_T = 40mΩ are close enough for this stage of the design. The voltage needed on the supercapacitor stack when the DC/DC converter drops out is:

$$\begin{aligned} V_{C(UV)} &= \frac{(V_{UV})^2 + P_{IN} \bullet R_T}{V_{UV}} \\ &= \frac{2.7V^2 \bullet 20W \bullet 40m\Omega}{2.7V} \\ &= 3V \end{aligned}$$

The require capacitance of the stack is:

$$C_{MIN} = \frac{2 \bullet P_{IN} \bullet T_{BU}}{(V_{C(0)})^2 - V_{C(UV)}} = \frac{2 \bullet 20W \bullet 45s}{4.8^2 - 3^2} = 128F$$

A stack of two 360F supercapacitors (NessCap ESHSR-0360C0-002R7A) have an end-of-life capacitance of 126F. The initial ESR is specified at 3.2mΩ with an end of life ESR at 6.4mΩ.

The crossover switch consists of an LTC4412 PowerPath™ controller and two Si4421DY, P-channel MOSFETs from Vishay. The $R_{DS(ON)}$ of the Si4421DY with a gate voltage of 2.5V is 10.75mΩ (max).

Using the values for the end of life ESR of the supercapacitors and the actual MOSFET's $R_{DS(ON)}$, the maximum interconnect resistance can be determined:

$$\begin{aligned} R_{DIST(MAX)} &= R_T - (2 \bullet ESR_{EOL} + R_{DS(ON)}) \\ &= 40m\Omega - (2 \bullet 6.4m\Omega + 10.5m\Omega) \\ &= 16.45m\Omega \end{aligned}$$

The LTC3625 has two configuration modes of operation. A single inductor configuration is used for supercapacitor charging currents of less than 0.5A and a dual inductor configuration for charging currents up to 1A. For this application, the 2-inductor configuration is used to meet the recharging time requirement with the 360F supercapacitors.

To determine the value for R_{PROG}, the stack capacitance is estimated at the supercapacitors initial capacitance plus the high side (20%) of its tolerance. From the graph in Figure 2, the charge time from 3V to 5.3V was estimated at 32 seconds.

$$\begin{aligned} R_{PROG} &= 143k \bullet \frac{10F}{360F \bullet 1.2} \bullet \frac{5.3V - 3V}{4.8V - 3V} \bullet \frac{600s}{32s} \\ &= 79.3k \end{aligned}$$

The nearest standard 1% resistor is 78.7k.

The initial start-up time is estimated at:

$$\begin{aligned} T_{STARTUP} &= 70s \bullet \frac{4.8V}{5.3V} \bullet \frac{360F \bullet 1.2}{10F} \bullet \frac{78.7k}{143k} \\ &= 1507s \end{aligned}$$

The data sheet suggests a 3.3µH inductor (Coilcraft MSS7341-332NL) for both the buck and boost inductors.

The LTC3625 contains a power fail comparator, which is used to monitor the input power to enable the LTC4412 PowerPath controller. The PFO comparator has an internal reference of 1.2V connected to the comparator's negative input. A voltage divider connected to the PFI pin sets the power fail trigger point (V_{PF}) to 4.75V. The bottom resistor is set to 100k, so the upper resistor is:

$$\begin{aligned} R_{UPPER} &= \frac{V_{PF} - V_{REF}}{V_{REF}} \bullet R_{LOWER} \\ &= \frac{4.75V - 1.2V}{1.2V} \bullet 100k \\ &= 295.8k \end{aligned}$$

The nearest standard 1% resistor is 294k.

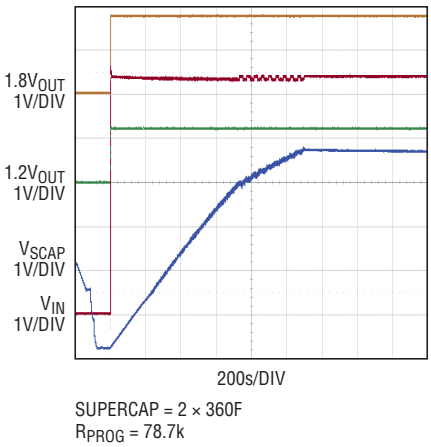


Figure 3. Initial charging of a depleted series connected pair of 360F supercapacitors

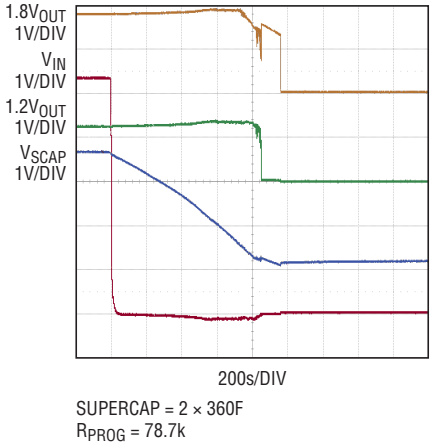


Figure 4. Supercapacitor backup time supporting a 20W Load

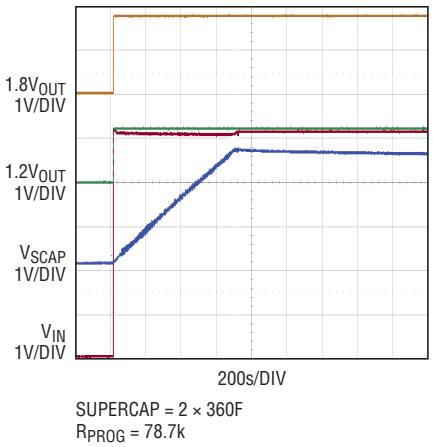


Figure 5. Recharge of series-connected pair of 360F supercapacitors

THE CIRCUIT IN ACTION

Figure 1 shows a complete supercapacitor energy storage system consisting of the LT33625, two Coilcraft 3.3µH inductors and two 360F supercapacitors from NessCap. The LTC4412 and the two Vishay Si4421DY MOSFETs make up the automatic crossover switch while the LTM4616 is the DC/DC converter that represents the constant power load to the energy storage system.

Figure 3 shows an initial charging time of 1112 seconds for the LTC3625 charging circuit. Using nominal component values the initial charging time is 1255 seconds, which is well within component tolerance levels. During the first 250 seconds, only the buck converter is charging the bottom supercapacitor and once the voltage reaches 1.35V, the boost converter starts to operate. Both the buck converter and the boost converter continue to operate for the next 500 seconds. An interesting observation of the charging profile is that after 750 seconds, the change in slope and the ripple voltage on the input voltage is due to the buck converter turning off and on during the final minutes of charging.

Figure 4 shows the backup time of the system with a 20W load. The desired backup time was 45 seconds while our system is supporting the load for 76.6 seconds. The longer available backup time is due to lower than estimated parasitic circuit resistances and that the DC/DC converters continue to operate down to 2.44V instead of the 2.7V in the design calculations. The output of the 1.8V converter can be seen to turn back on again when the 1.2V converter turns off. This "motor-boating" effect is caused by the rise in voltage at the input of the DC/DC converter when the input current is reduce as the 1.2V converter section turns off. This can be eliminated by adding an external undervoltage lockout circuit with adequate hysteresis to disable the DC/DC converter.

Finally, Figure 5 shows the recharge time of the supercapacitors after a backup operation. The recharge time is actually 685 seconds, compared to the 600 seconds used in the calculations. The longer charging time is attributed to the lower starting voltage of 2.44V for the DC/DC converter.

CONCLUSION

Supercapacitors are replacing batteries to satisfy green initiative mandates for data centers. The LTC3625 is an efficient 1A supercapacitor charger with automatic cell balancing that can be combined with the LTC4412 low loss PowerPath controller to produce an energy storage system that protects data in RAID disk applications. The LTC3625 is available in a 12-lead 3mm × 4mm × 0.75mm DFN package. ■

True Grid Independence: Robust Energy Harvesting System for Wireless Sensors Uses Piezoelectric Energy Harvesting Power Supply and Li-Poly Batteries with Shunt Charger

George H. Barbehenn

There is an emerging and potentially large market for wireless sensors. By their very nature, wireless sensors are chosen for use in inaccessible places, or for applications that require large numbers of sensors—too many to easily hardwire to a data network. In most cases, it is impractical for these systems to run off primary batteries. For example, a sensor for monitoring the temperature of meat as it is shipped would need to be mounted in a tamperproof way. Or, HVAC sensors that are mounted on every source of conditioned air would be far too distributed to feasibly use batteries. In these applications, energy harvesting can solve the problem of providing power without primary batteries.

Energy harvesting alone often does not produce sufficient power to continuously run the sensor-transmitter—energy harvesting can produce about 1mW–10mW, where the active sensor-transmitter combination may need 100mW–250mW. Harvested energy must be stored when possible, ready for use by the sensor/transmitter, which must operate at duty cycle that does not exceed the energy storage capabilities of the system. Likewise, the sensor/transmitter may need to operate at times when no energy is harvested.

Finally, if the stored energy is depleted and the system is going to shut down, the system may need to carry out housekeeping tasks first. This may include a shutdown message, or storing information in nonvolatile memory. Thus, it is important to continuously gauge available energy.

COMPLETE ENERGY HARVESTING SYSTEM

Figure 1 shows a complete system implementation using an LTC3588-1 energy harvester and buck regulator IC, two LTC4071 shunt battery chargers, two GM BATTERY GMB301009 8mAh batteries and a simulated sensor-transmitter modeled as a 12.4mA load with 1% duty cycle. The LTC3588-1 contains a very low leakage bridge rectifier with

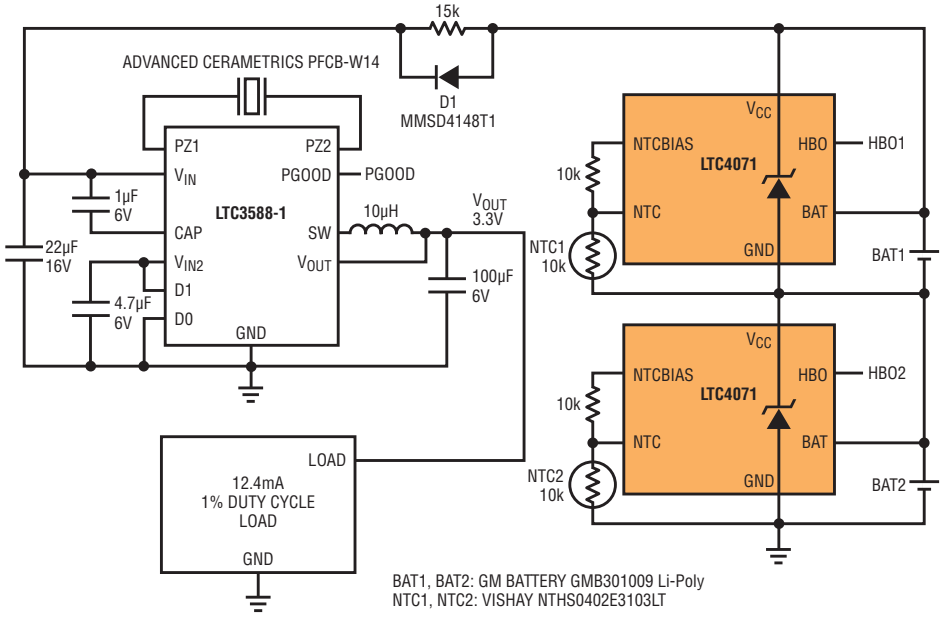


Figure 1. Complete piezo-based energy harvesting system is independent of the grid. This design uses thin film batteries to gather energy collected by the piezo for a wireless sensor transmitter, which operates on a 1% duty cycle.

With a few easy-to-use components, it is possible to build a complete compact energy-harvesting power subsystem for wireless sensor-transmitters.

inputs at PZ1 and PZ2 and outputs at V_{IN} and GND. V_{IN} is also the input power for a very low quiescent current buck regulator. The output voltage of the buck regulator is set by D1 and D0 to 3.3V.

The LTC3588 is driven by an Advanced Cerametrics Incorporated PFCB-W14 piezoelectric transducer, which is capable of generating a maximum of 12mW. In our implementation, the PFCB-W14 provided about 2mW of power.

The LTC4071 is a shunt battery charger with programmable float voltage and temperature compensation. The float voltage is set to 4.1V, with a tolerance on the float voltage of ±1%, yielding a maximum of 4.14V, safely below the maximum float allowed on the batteries. The LTC4071 also detects how hot the battery is via the NTC signal and reduces the float voltage at high temperature to maximize battery service life.

The LTC4071 is capable of shunting 50mA internally. However, when the battery is below the float voltage, the LTC4071 only draws ~600nA of current from the battery.

The GM BATTERY GMB301009 batteries have a capacity of 8mAh and an internal series resistance of ~10Ω.

The simulated sensor-transmitter is modeled on a Microchip PIC18LF14K22 and MRF24J40MA 2.4GHz IEEE standard 802.15.4 radio. The radio draws 23mA in transmit and 18mA in receive. The model represents this as a 12.4mA, 0.98% duty cycle (2ms/204ms) load,

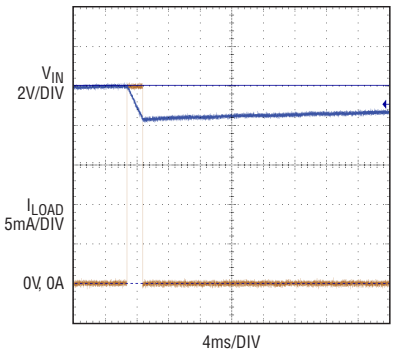


Figure 2. Charging with sensor-transmitter load

set with a self-clocked digital timer and a MOSFET switching a 267Ω resistor.

MODES OF OPERATION

This system has two modes of operation: charging-sending and discharging-sending. In charging-sending mode, the batteries are charged while the sensor-transmitter presents a 0.5% load. When discharging, the sensor-transmitter is operating, but no energy is being harvested from the PFCB-W14.

Charging-Sending

When active, the PFCB-W14 delivers power at an average of approximately 9.2V × 180µA ≈ 1.7mW. The available current must charge the battery and operate the buck regulator driving the simulated sensor-transmitter. The active sensor-transmitter draws 12.4mA × 3.3V ≈ 41mW at around 1% of the time, or about 0.41mW on average, leaving some current to charge the battery. Taking into account the 85% efficiency of the LTC3588 buck regulator, assuming an average V_{IN} of 9.2V (see Figure 2), and a buck quiescent current of 8µA, the average current consumed by the system without charging the battery is:

$$I_{AVG} = \frac{I_{SENSOR}}{\frac{V_{IN(AVG)}}{V_{OUT}} \bullet \eta_{BUCK}} \bullet DUTYCYCLE + I_{Q(BUCK)}$$

$$I_{AVG} = \frac{12.4mA}{\frac{9.2V}{3.3V} \bullet 0.85} \bullet 0.0098 + 8\mu A \cong 60\mu A$$

Harvested energy can drive the sensor-transmitter at a 0.5% duty cycle with about 120µA left to charge the batteries. The GMB301009 batteries have a capacity of 8mAh, so they completely charge from empty in about 75 hours.

Discharging-Sending

When the PFCB-W14 is not delivering power, the voltage at V_{IN} drops to approximately:

$$\frac{8.4 + 6.6}{2} = 7.5V$$

So the reflected load current calculation changes to:

$$I_{AVG} = \frac{12.4mA}{\frac{7.5V}{3.3V} \bullet 0.85} \bullet 0.0098 + 15\mu A \cong 78\mu A$$

The quiescent current of the buck regulator is higher because the regulator must switch more often to regulate from 7.5V versus 9.2V. At 78µA, with no energy harvested, the battery is discharged in approximately 115 hours. This indicates a charge storage capacity of >8.95mAh. These batteries when brand new could store approximately 12% more charge than rated.

A more serious problem is what happens when the battery is fully discharged. If current is drawn after the state of charge reaches zero, and the battery voltage drops

below 2.1V, the battery is permanently damaged. Therefore the application must ensure that the battery voltage never falls below this limit. For this reason, the battery cutoff voltage is set to 2.7V or 3.2V to ensure some energy remains in the battery after the disconnect circuit has engaged.

Simply stopping the transmitter or disconnecting the load will not protect the battery, as the LTC4071 draws a quiescent current of approximate 600nA. Although this is extremely low, the total load, including the LTC3588-1, is nearly 2µA. A fully discharged battery will only be able to supply approximately 100µA before its voltage drops enough to damage the battery.

A disconnect circuit is necessary to ensure that the battery does not discharge in a reasonable amount of time. The LTC4071 provides an internal low battery disconnect circuit. This disconnect circuit was measured to provide <2nA of battery load at room temperature when activated. This leakage is typically dominated by PCB leakage. With only 2nA of battery drain current, the battery could survive for 50,000 hours in the disconnect state before the battery is damaged.

In Figure 3, the second battery (BAT2) is seen to disconnect 50 hours after BAT1 due to the 2µA load.

MEASURED RESULTS

The system shown in Figure 1 was measured in both operating modes discharging-sending (Figure 3) and charging-sending (Figure 4).

Discharging-Sending

In Figure 3 the voltages of the two batteries BAT1, BAT2 and V_{BUCK} are plotted against time with the batteries supplying all the system energy, none from the PFCB-W14 piezo.

The batteries slowly discharge until BAT2 activates the LBO threshold of the LTC4071, whereupon the disconnect circuit activates and disconnects BAT2 from all circuitry except U5. This causes the voltage at V_{IN} of the LTC3588 to drop below the UVLO for the regulator, and the regulator shuts off.

The load on BAT1 is the 2µA quiescent current of the LTC4071 and the LTC3588. This small load slowly discharges BAT1 until the low battery disconnect of LTC4071 is activated and BAT1 is disconnected.

Charging-Sending

When the PFCB-W14 once again starts delivering power to the system, V_{IN} rises to 7V, which forward biases the body diodes of the disconnect FETs in the LTC4071. This charges the batteries until the reconnect threshold is reached, allowing batteries BAT1 and BAT2 to be reconnected. Looking at Figure 4, this can be seen as the voltage at V_{IN} snaps down to the battery stack voltage.

Since the voltage at V_{IN} is now V_{BAT1} + V_{BAT2} + (180µA × 15k) = 6.2V, the buck regulator on the LTC3588 restarts and 3.3V is once again available.

CONCLUSION

With a few easy-to-use components, it is possible to build a complete compact energy-harvesting power subsystem for wireless sensor-transmitters. In this particular system a piezoelectric transducer supplies intermittent power, while two batteries store energy for use by the sensor-transmitter. An integrated disconnect switch protects the batteries from overdischarge.

This system can fully charge the battery in 75 hours, even while operating the sensor-transmitter at 0.5% duty cycle.

The batteries allow the system to continue operating the sensor-transmitter at 0.5% duty cycle for 115 hours after the PFCB-W15 stops providing power. If longer battery operating time is required, the sensor-transmitter duty cycle can be reduced to accommodate this need. ■

Figure 3. Discharge with battery undervoltage disconnect

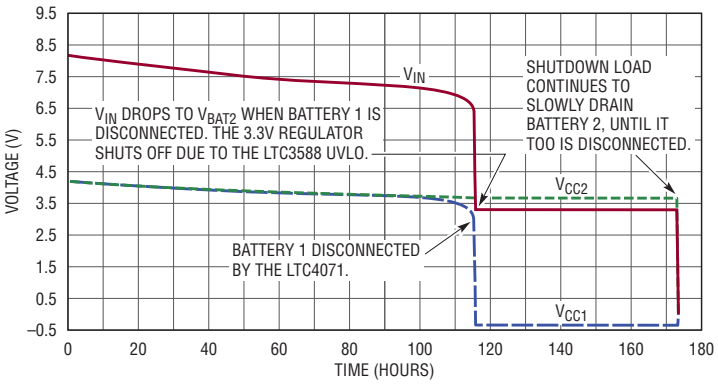
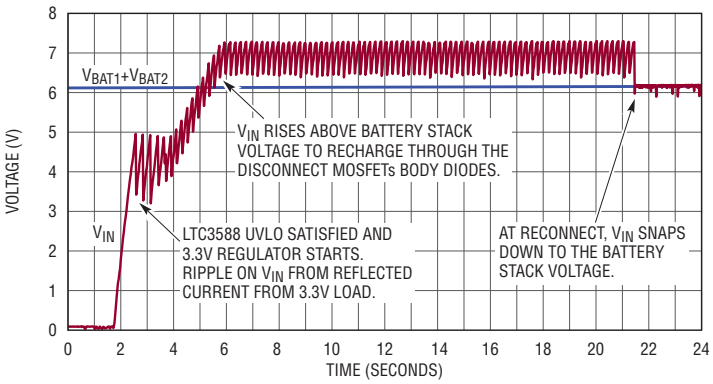


Figure 4. Battery disconnect recovery on charge



Passive Mixers Increase Gain and Decrease Noise When Compared to Active Mixers in Downconverter Applications

Tom Schiltz, Bill Beckwith, Xudong Wang and Doug Stuetzle

The LTC554x family of passive downconverting mixers covers frequencies from 600MHz to 4GHz and delivers high conversion gain and low noise figure (NF) with high linearity. These mixers are targeted at wireless infrastructure receivers that require a high gain mixer to overcome the high insertion loss of today's high selectivity IF SAW filters. While legacy passive mixers typically have 7dB of conversion loss, the new LTC554x mixers have integrated IF amplifiers, as shown in Figure 1, which produce 8dB of overall conversion gain. This allows an additional 15dB of IF filter loss, while still enabling the receiver to meet sensitivity and spurious-free dynamic range requirements.

Figure 1. LTC554x passive mixer in a receiver application

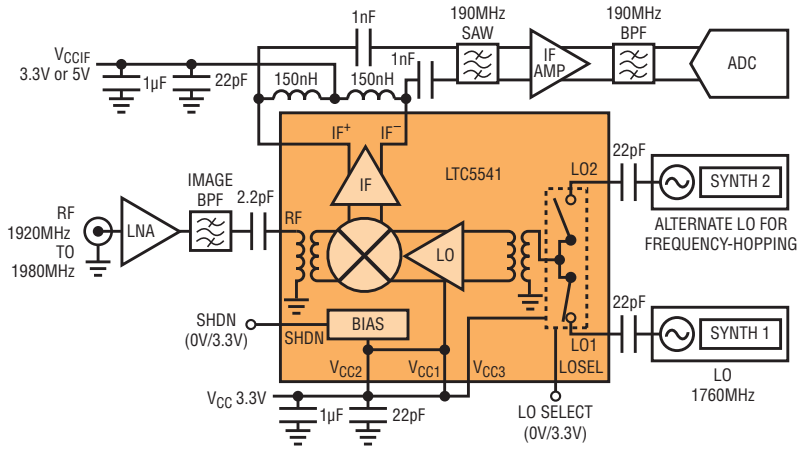


Table 1. Active vs passive mixer comparison at 1.95GHz

PART	GAIN (dB)	NF (dB)	IIP3 (dBm)	INPUT P1dB (dBm)	DC POWER (mW)
LTC5541 (passive)	7.8	9.6	26.4	11.3	630
LT5557 (active)	2.9	11.7	24.7	8.8	270

ACTIVE VERSUS PASSIVE MIXERS

Most integrated-circuit mixers are based on an active or current-commutating topology. Linear Technology has a wide portfolio of active mixers, such as the LT5527 and LT5557, which are widely accepted due to their ease of use and low power consumption. Nevertheless, their 2dB–3dB of conversion gain is not enough for some wireless infrastructure designs. Furthermore, active mixers typically exhibit higher NF than passive mixers at comparable linearity. LTC554x mixers employ a passive mixer core to achieve the lowest NF with high linearity. Table 1 compares the performance of the LTC5541 passive mixer to the LT5557 active mixer. As shown in the table, the passive mixer has approximately 5dB higher gain, 2dB lower NF and 1.7dB higher IIP3. The LT5557, though, has much lower DC power consumption.

LARGE-SIGNAL NOISE FIGURE

Another important mixer performance parameter is large-signal noise figure. As in an amplifier, the NF of a mixer is the ratio of the input S/N to the output S/N. All mixers suffer from increased NF when driven with high level RF signals. This phenomenon is also referred to as "noise figure under blocking" in receiver applications, where the "blocking" signal is a high amplitude signal in an adjacent channel. Elevated noise figure occurs because the mixer's output noise floor is proportional to the RF input amplitude multiplied by the LO path noise ($A_{RF} \bullet N_{LO}$).

The new LTC554x family of passive downconverting mixers delivers the high performance that is needed for today's wireless infrastructure receivers.

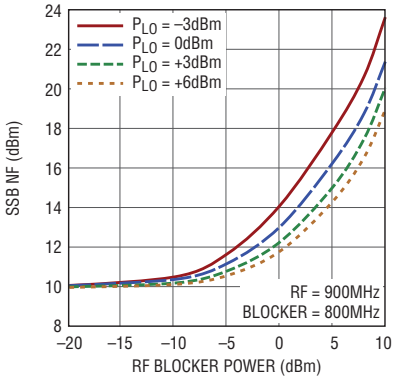


Figure 2. LTC5540 noise figure vs RF blocker level

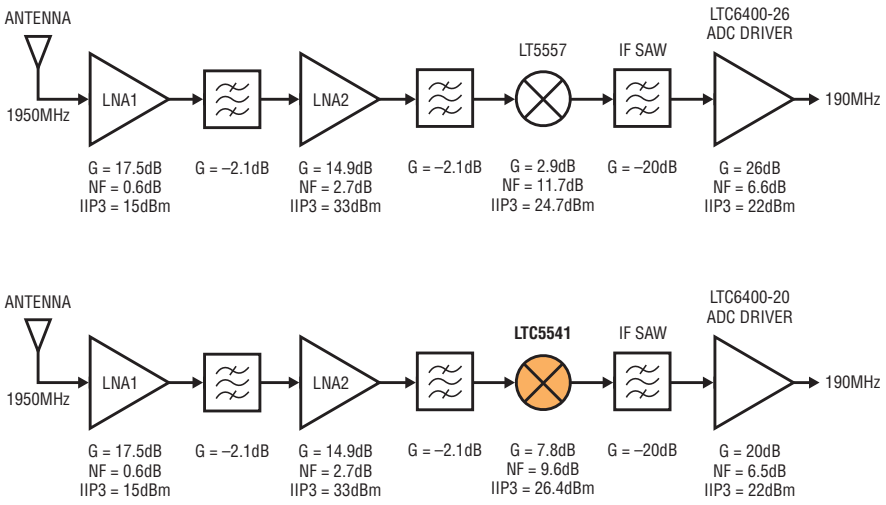
PART	RF FREQUENCY (MHz)	LO INJECTION	SMALL-SIGNAL NF (dB)	LARGE-SIGNAL NF (dB)
LTC5540	900	High-Side	9.9	16.2
LTC5541	1950	Low-Side	9.6	16.0
LTC5542	2400	Low-Side	9.9	17.3
LTC5543	2500	High-Side	10.2	17.5

Table 2. LTC554x large-signal noise figure with +5dBm blocker

There are many times when a receiver needs to detect a weak signal in the presence of strong blocker. If the blocker causes the noise floor to rise sufficiently, then the desired weak signal could be lost in the noise. Figure 2 shows NF vs RF input power for the LTC5540. The NF approaches the small-signal value at low input levels, but as the RF signal power is increased, the $A_{RF} \bullet N_{LO}$ contribution becomes dominant, and the NF increases. With a high RF input level of +5dBm, and a nominal LO power of 0dBm, the NF increases only 6dB from the small-signal value, to 16.2dB. It is also apparent from the graph that the large-signal noise improves with higher LO power level, thus even better performance can be realized if necessary.

While elevation of the noise figure cannot be totally eliminated, performance can be improved through careful design. All of the parts in the LTC554x family exhibit excellent large-signal noise figure behavior, as shown in Table 2.

Figure 3. Typical wireless basestation receiver line-up comparison of a LT5557-based receiver and a LTC5541-based receiver



CASCADED RECEIVER PERFORMANCE SUMMARY

LINE-UP	GAIN (dB)	NF (dB)	IIP3 (dBm)
LT5557-BASED	35.0	4.03	–1.6
LTC5541-BASED	33.9	3.27	0.0

The combination of high conversion gain, low NF, excellent NF under blocking and high linearity can improve overall system signal-to-noise ratio and SFDR. The excellent performance also contributes to improved DPD receiver performance.

CALCULATED PERFORMANCE COMPARISON IN A RECEIVER CHAIN

The benefits of these new passive mixers are demonstrated in the following receiver chain analysis. A typical, single-conversion basestation receiver line-up is shown in Figure 3 and is used to compare the overall system performance when the LT5557 active mixer is used to the same receiver using the new LTC5541 passive mixer. The LTC6400-26 IF amplifier, with 26dB of gain, is used with the 5557-based line-up, and LTC6400-20, with 20dB of gain, is used with the 5541-based line-up. This keeps the overall receiver gain nearly the same for both cases. A high selectivity SAW filter is used at the mixer's output in each case, as required by the high performance basestation. As shown in Figure 3, the receiver line-up using the LTC5541 passive mixer has 0.76dB lower NF and 1.6dB higher IIP3. This results in higher signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) for the 5541-based receiver.

MEASURED PERFORMANCE COMPARISON IN A TRANSMITTER DPD APPLICATION

In its simplest form, a single-conversion digital receiver consists of a downconverting mixer, a lowpass or bandpass filter, and an analog-to-digital converter (ADC). This type of receiver can be used as a digital pre-distortion (DPD) receiver in high linearity basestation transmitters. In this application, the most important performance parameters are linearity, gain flatness, wide IF bandwidth and, of course, simplicity. Unlike the receiver application described earlier, NF is not critical in DPD applications due to the high amplitude signal coupled from the transmitter output. The LTC554X mixers are ideal candidates for use in DPD receiver applications due to their high linearity, high conversion gain and flat IF output response versus frequency.

A prototype DPD receiver using the LTC5541 is shown in Figure 4. This receiver was built and tested for a 1.95GHz application with a wideband IF of 185 ± 60MHz.

For comparison, another receiver was built using the LT5557 active mixer. The 5557-based DPD receiver required an external IF amplifier preceding the bandpass filter to make up for the 5dB lower gain of the active mixer. The primary advantage of the LTC5541 is that it eliminates the need for this IF amplifier. Furthermore, as summarized in Table 3, the 5541-based DPD receiver delivered a higher SNR, higher IIP3 and lower harmonic distortion.

CONCLUSION

The new LTC554X family of passive downconverting mixers delivers the high performance that is needed for today's wireless infrastructure receivers. The mixers' combination of high conversion gain, low NF, excellent NF under blocking and high linearity can improve overall system signal-to-noise ratio and SFDR. The excellent performance also contributes to improved DPD receiver performance while the 600MHz to 4GHz frequency coverage of the LTC554X family makes them useful in a wide variety of receiver applications. ■

Figure 4. Prototype DPD receiver block diagram

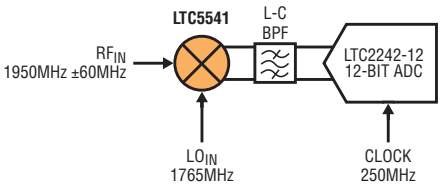


Table 3. Prototype DPD receiver measured results (RF = 1950MHz, IF = 185MHz)

MIXER	0.5dB IF BW	INPUT LEVEL AT –1dBFS	SNR AT –1dBFS	HD2 AT –7dBFS	IM3 AT –7dBFS
LTC5541	126MHz	–0.6dBm	63.4dB (120MHz)	–54.5dBc @ 123MHz –78.2dBc @ 184MHz –69.5dBc @ 243MHz	–64.8dBc
LT5557	130MHz	–1.8dBm	62.8dB (120MHz)	–52.4dBc @ 123MHz –63.1dBc @ 184MHz –67.4dBc @ 243MHz	–58.0dBc

Product Briefs

PRECISION SUPPLY SUPERVISOR WITH POWER-FAIL COMPARATOR

The LTC2911 is a family of five precision triple supply monitors featuring a tight 1.5% threshold accuracy over the entire operating temperature range. Each member of the family provides the ability to monitor three supply voltages and generate a system reset when any of the voltages are out of compliance. Additionally, an early warning power-fail comparator is available providing an early indication that input power may be going away.

Three 5% supplies may be monitored via the V1, V2 and ADJ input pins. For most applications, no external resistors are required for V1 and V2. The V1 threshold is fixed for monitoring a 3.3V supply, while the V2 threshold varies with the part number; 5V for LTC2911-1, 2.5V for LTC2911-2, 1.8V for LTC2911-3 and 1.2V for LTC2911-4 (see Table 1). The ADJ pin has a threshold of 0.5V and may be connected to an external resistive divider to monitor an arbitrary supply voltage. For the LTC2911-5, the V2 input becomes a second adjustable input (0.5V threshold) allowing two arbitrary supply voltages to be monitored. Power to the LTC2911 comes from the higher of the V1 and V2 monitor inputs, the exception being the LTC2911-5 which derives its power only from V1.

Each supply monitor features a power-fail comparator which provides an early warning of a low voltage condition to allow a system to take preemptive action before the power fails completely. The power-fail comparator has a falling threshold of 0.5V and a rising threshold of 0.515V, giving a 3% hysteresis for noise rejection. The hysteresis may also be increased by adding two external resistors.

The LTC2911 provides two status outputs, PFO and RST, which are both open drain outputs with weak internal pull-ups to V1. These pins can be pulled to higher voltages by external resistors. PFO is the output of the power-fail comparator and pulls low if the power-fail input, PFI, is low. When the V1, V2 and ADJ supplies are all above their respective thresholds, a reset timer is started, and on timeout, RST is pulled high. To monitor more than three supplies, the RST pins of multiple LTC2911s can be connected to form a wire-OR.

The timeout period depends on how the TMR pin is configured. Tying TMR high forces an internally generated timeout period of 200ms without the need for an external timing capacitor.

The timeout period can also be set to 9.4ms/nF by connecting an external capacitor from TMR to ground.

The TMR pin has a latch feature (activated by pulling TMR low) to latch in the high state of RST so that margin testing can be performed without causing the system to reset. Once the tests are done, the supplies are returned to their normal levels and the TMR is allowed to float or be pulled high to release the latch. When any of the V1, V2 or ADJ supplies are below their respective thresholds, RST pulls low until all three supplies go high and the timer times out.

The LTC2911 family includes built-in glitch filters to prevent spurious or nuisance resets. Additional filtering may be added by connecting capacitors from V2 (LTC2911-5), ADJ and PFI to ground.

The power-fail comparator allows early detection of supply outages, and the

Table 1. LTC2911 triple supply monitor family

PART NUMBER	PACKAGE DESCRIPTION	V1	V2
LTC2911-1	8-Lead (3mm × 2mm) Plastic DFN	3.3V	5V
LTC2911-2	8-Lead (3mm × 2mm) Plastic DFN	3.3V	2.5V
LTC2911-3	8-Lead (3mm × 2mm) Plastic DFN	3.3V	1.8V
LTC2911-4	8-Lead (3mm × 2mm) Plastic DFN	3.3V	1.2V
LTC2911-5	8-Lead (3mm × 2mm) Plastic DFN	3.3V	ADJ
LTC2911-1	8-Lead Plastic TSOT-23	3.3V	5V
LTC2911-2	8-Lead Plastic TSOT-23	3.3V	2.5V
LTC2911-3	8-Lead Plastic TSOT-23	3.3V	1.8V
LTC2911-4	8-Lead Plastic TSOT-23	3.3V	1.2V
LTC2911-5	8-Lead Plastic TSOT-23	3.3V	ADJ

Each LTC2911 supply monitor features a power-fail comparator which provides an early warning of a low voltage condition to allow a system to take preemptive action before the power fails completely.

ability to latch the RST state makes it easy to run supply margining tests.

External component count is minimal. No timer capacitor is needed to generate a 200ms timeout. The small SOT-23 and DFN packages save board space. All these features make the LTC2911 a compelling choice for systems that need to monitor three or more supplies.

The LTC2911 is available in space saving 8-lead TSOT-23 and 3mm × 2mm DFN packages.

SUPPLY PROTECTION CONTROLLER GUARDS AGAINST OVERVOLTAGE, UNDERVOLTAGE AND REVERSE POLARITY FAULTS

The LTC4365 is an overvoltage (OV), undervoltage (UV) and reverse protection controller, with a –40V to 60V protection range, for applications that require windowed supply protection. The LTC4365 provides two comparator inputs to configure the OV and UV set points within the normal operating range of 2.5V to 34V using an external resistive divider. A gate pin controls a dual N-channel MOSFET to ensure only voltages within the OV and UV window are passed to the output. Reverse supply protection circuits automatically isolate the load from negative input voltages. In addition to providing transient protection to 60V, the LTC4365 also blocks 50Hz and 60Hz AC power. No TVS or input capacitor is required for most applications, providing a low component count solution for compact designs.

The LTC4365 consumes only 125µA in normal operation, and has a shutdown pin for enabling and disabling the external MOSFETs, and for providing a low current shutdown state of 10µA. A fault output indicates gate status. Using the shutdown pin, two LTC4365's can be configured in a novel application to select between two power supplies. If reverse protection is not needed, only a single external MOSFET is required.

The LTC4365 is offered in 8-pin (3mm × 2mm) DFN and TSOT-23 packages.

HOT SWAP CONTROLLER WITH INTEGRATED 5A MOSFET AND R_{SENSE}

The LTC4219 5A Hot Swap™ controller protects low power boards with load supply voltages ranging from 2.9V to 15V. The LTC4219 allows a board to be safely inserted and removed from a live backplane by limiting the amount of inrush current to the load supply during power up. Hot Swap controllers typically call for a number of supporting components. However, the LTC4219 integrates a power MOSFET and sense resistor in its power path to limit inrush current, reducing the number of external components required. The device's internal dv/dt circuit means there is no need for an external gate capacitor. An adjustable current limit allows users to vary the current limit threshold under different loading conditions, for example in disk drive spin-up to normal operation. This high level of integration, packaged in a tiny DFN, makes the LTC4219 a convenient Hot Swap solution in space-constrained applications.

The LTC4219 is suitable for a wide range of RAID, server, telecom and industrial applications, especially in compact boards utilizing technologies like Fibre Channel where power is typically limited to less than 25W due to their small size and inability to dissipate large amounts of heat. The LTC4219 was designed with these considerations in mind.

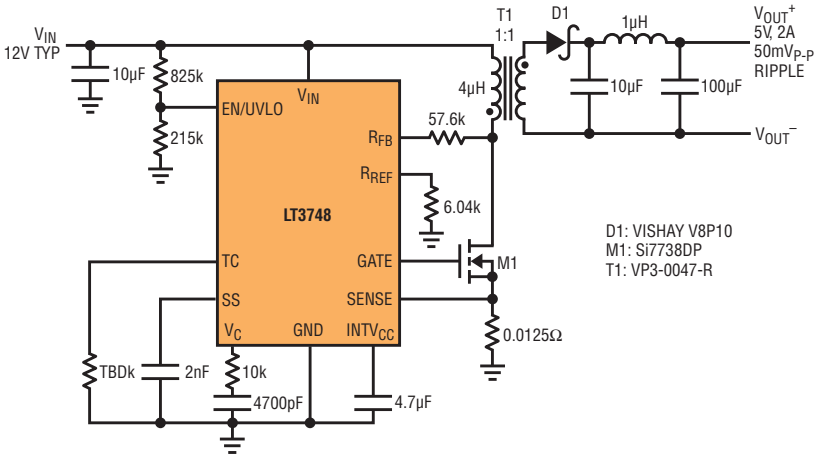
During start-up, inrush currents are controlled by limiting the gate ramp rate to a safe 0.3V/ms. Load current is monitored using the voltage sensed across the internal 7.5mΩ sense resistor and adjusting the internal 33mΩ MOSFET gate-to-source voltage accordingly. A separate I_{SET} pin enables adjustment of the 10% accurate (5A) current limit threshold during start-up and normal operation as needed. In addition, current foldback and power good circuitry ensure that the switch is protected from excessive load current and indicate whether or not healthy power conditions are maintained. The LTC4219 also features current, temperature and fault outputs, as well as an adjustable current limit timer.

The LTC4219 is available as a dedicated 12V (LTC4219-12) or 5V (LTC4219-5) version, which contain preset 12V/5V-specific thresholds. The LTC4219 is available in a small, RoHS-compliant, 16-pin 5mm × 3mm DFN package. ■

5V, 2A OUTPUT FROM AUTOMOTIVE INPUT WITH CONTINUOUS OPERATION FROM 6V TO 45V

The LT3748 is a switching regulator controller specifically designed for the isolated flyback topology and capable of high power. No third winding or opto-isolator is required for regulation as the part senses the isolated output voltage directly from the primary-side flyback waveform. The gate drive of the LT3748 combined with a suitable external MOSFET allow it to deliver load power up to several tens of watts from input voltages as high as 100V.

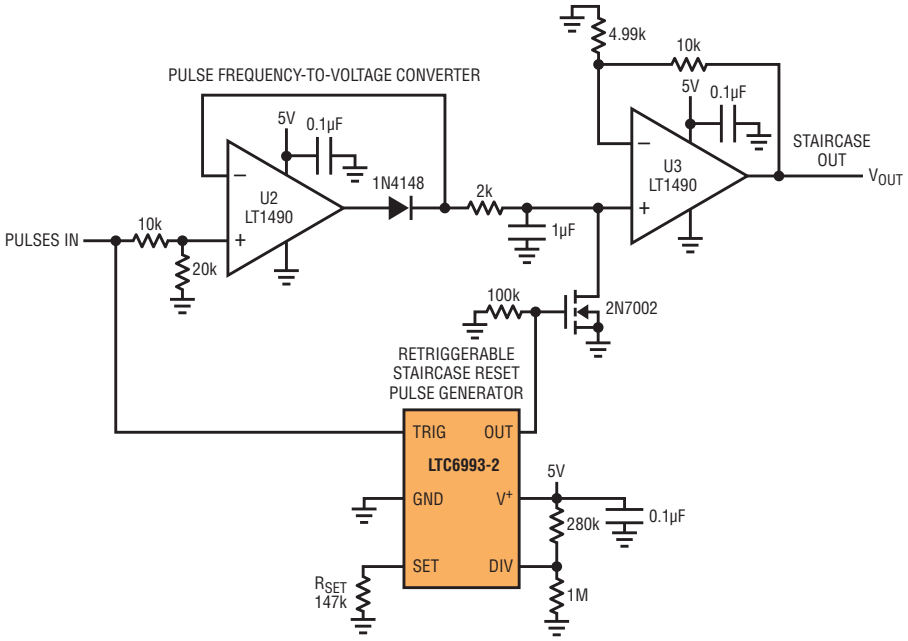
www.linear.com/3748

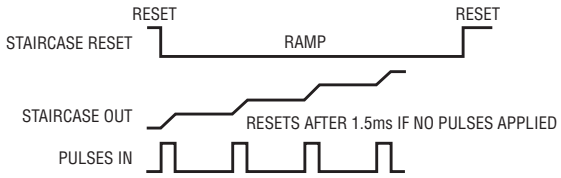


PULSE FREQUENCY-TO-VOLTAGE CONVERTER

The LTC6993 is a monostable multivibrator (also known as a "one-shot" pulse generator) with a programmable pulse width of 1µs to 33.6 seconds. The LTC6993 is part of the TimerBlox™ family of versatile silicon timing devices. A single resistor, R_{SET}, programs the LTC6993's internal master oscillator frequency. The output pulse width is determined by this master oscillator and an internal clock divider.

www.linear.com/6993





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